0.3V Biopotential Sensor Interface for Stress Monitoring

by

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B.S., Electrical Engineering, Middle East Technical University (2013)

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

Master of Science in Electrical Engineering and Computer Science

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

June 2016

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Abstract

Miniaturized sensor nodes have a very tight power budget, especially in the case of implantables and health monitoring devices that require long operation lifetime. Exploiting low-voltage techniques in analog design can enable further power savings, which has not been explored much. However, for conventional analog-front-end (AFE) topologies, voltage scaling could potentially bring several limitations to the important performance metrics such as the linearity, robustness and the power-efficiency. This thesis work describes the design of a $0.3V$ biopotential sensor interface for stress monitoring applications, which achieves state-of-the-art power-efficiency, and ensures enough circuit reliability with reduced dynamic range requirement.

The proposed sensor interface consists of an amplifier and an analog-to-digital converter (ADC). The simulated amplifier achieves $0.95nW$ power consumption with a power-efficiency-factor (PEF) of 1.57. With this power budget, the amplifier also presents large signal cancellation capability in order to reject the motion artifacts. The system, together with the ADC consumes $4.1nW$ power, and has an area of $0.2mm^2$, which makes the sensor interface suitable for wearable and implantable devices. The chip has been submitted for fabrication in a low power $65nm$ digital CMOS process, and the simulation results are presented.

Thesis Supervisor: Anantha P. Chandrakasan
Title: Vannevar Bush Professor of Electrical Engineering and Computer Science

Acknowledgments

This thesis would not have been possible without the support and help of an endless list of colleagues, friends and family. First and foremost, I would like to thank my research supervisor, Professor Anantha Chandrakasan. Your vision, encouragement and your guidance has been invaluable for my research. It is very inspiring to see how you take care of each of us, and make each of our experience at MIT unique. I am very grateful for all your support.

Next, I would like to thank Harneet Singh Khurana for his contributions to the project by designing the ADC block. I feel very fortunate to be able to work with a colleague with such positive energy and motivation to explore new challenges. I also would like to thank Professor Hae-Seung Lee for sharing his expertise on analog design, and providing us feedback at the most critical stages of the project.

I also owe a debt of gratitude to Frank Yaul for his mentorship. You have helped me at every stage of this project starting from day one. As an expert in the field, as a perfectionist and as a friend, I have learned a lot from you. Thank you for all your effort and time you dedicated to this project, as well as for your sincerity.

I would also like to thank Arun Paidimarri and Phil Nadeau. Whenever I have been stuck, no matter what the problem is, no matter what time of the day it is, you have always been there to help me. The level of devotion and enthusiasm you have put to your work is rare to find. Thank you for being a source of inspiration for all of us.

To all of the Ananthagroup members: It has been a great experience for me to work with you. A group with such diversity of cultures and technical backgrounds, but all them having the same goal of making the most of their time at MIT. I feel very fortunate to be surrounded by such energetic people in the lab. Special thanks to Preet, Chu and Rabia. I would also like to thank Margaret for keeping everything in the lab running on time, and being always so responsive to us.

I also owe a very important debt to Dr. Konstantina Stankovic. The wide range of expertise you have in many interdisciplinary fields and your mentoring were very important for us to shape the application side of the project. Thank you very much

for being a role model for me.

I would also thank TSMC University Shuttle Program for the chip fabrication, and Siebel Foundation for my funding.

To my friends: Thanks to all my friends from childhood and from the university. It is so nice to see that no matter where we are, no matter how much our lives can diverge, we can still stay connected. I miss you, and hope to see you more often in the following years. Special thanks to Yunus for your love and support. Also, thank you to my Boston friends, namely WHP, who have made my experience in the last two years more fun and exciting. Even though each of us have their own crazy schedules, it is great to find time to disconnect from everything, and to spend time together.

And finally, I owe almost everything to my family. Your endless love and support in any decision I have taken has made me the person I am today. Thank you for always believing in me sharing every single moment of my life!

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Chapter 1

Introduction

In the recent years, the potential for advances in ultra-low-power electronics and sensors to improve the quality of medical care has led to surge of interest in miniaturized biomedical circuits. Miniaturization is important in the world of implantables and wearable sensor nodes, since the devices can reach to various locations in our body, and provide better comfort level for the patients. However, as the device sizes are getting smaller, the power that can be delivered is becoming limited. Considering the fact that the power available from a state-of-the-art 1 mm^3 solid-state thin-film battery is limited to 4 nW for a 10 year lifetime [6], researchers are motivated to explore systems that are able to operate at sub-uW power levels.

Biopotential signal acquisition systems such as electroencephalogram (EEG), electrocardiogram (ECG) and electromyogram (EMG) open a broad range of applications for these personalized medical devices, since they provide important information about certain health-related conditions of a person. However, designing wireless sensor nodes for monitoring these signals with such a low power budget is a nontrivial problem, which requires careful design both in analog and digital domain.

In order to better address the conceptual problem and the challenges, we need to know the definition of a sensor node and its components. A sensor node is a node in a

sensor network, which has the ability to sense and process the information as well as to communicate. As an example, we will consider a biomedical sensor node. Figure 1-1 shows an illustration, which has a low-noise-instrumentation amplifier for sensing, an analog-to-digital-converter (ADC) for digitization, a digital signal processing (DSP) block for processing the data. Once it is processed, the data can be stored and sent to a computer/phone wirelessly through a radio. Finally, the computer/phone can analyze the data, or send it to the medical server in order to inform the doctor about the patient's vital signs.

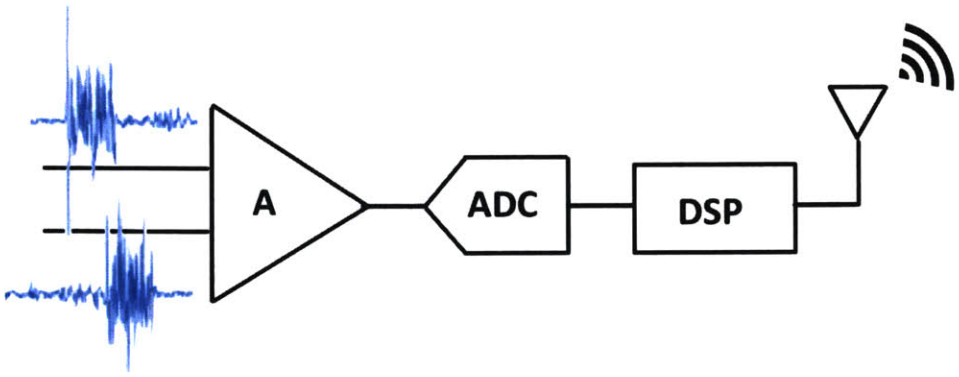

Figure 1-1: Main components of a biopotential sensor node.

The thesis will focus on the design and implementation of a 0.3V ultra-low-power biopotential analog-front-end (AFE), which achieves state-of-the-art power-efficiency, and ensures enough reliability for practical applications. The sensor interface has been designed specifically for EMG signals, and will be used for stress monitoring applications. The collected data throughout the project will be analyzed in order to provide diagnostic information about bruxism, temporomandibular joint disorder (TMJD), migraines and several other stress originated problems.

The remainder of the chapter will be divided as follows. Section 1.1 will give an overview of biopotential signal acquisition by explaining the origin and characteristics of the biopotentials signals, the target application, the requirements of the AFEs

and some examples from the state-of-the art designs. Section 1.2 will discuss the motivation for low voltage analog design. Section 1.3 will highlight the goals and contributions of the project. Finally, Section 1.4 will provide an outline for the thesis.

1.1 Biopotential Signal Acquisition

This section will discuss the signal characteristics of the biopotentials, the target application and some basic requirements of the AFEs. At the end of the section, we will give some examples from the state-of-the-art designs.

1.1.1 Biopotentials

Biopotentials are generated due to the electrochemical activity in certain class of cells that are components of the nervous or muscular tissue. Electrically, these cells generate action potentials in response to an electrical stimuli generated through the central nervous system. Different biopotential signals such as EEG, ECG, EMG are the results of several action potentials produced by different group of cells. For instance EEG measures the electrical activity in the brain, where as ECG measures the electrical activity in the heart. On the other hand, EMG signals are due to the electrical activity of the muscles during contraction.

Figure 1-2 shows magnitude and frequency characteristics for EEG, ECG and EMG signals, when they are measured with surface electrodes [1]. Even though the magnitude and frequency band of interest may slightly differ for each of them, all of them are low frequency signals that have extremely weak characteristics.

In addition to their extremely weak amplitude behavior, biopotentials are inevitably contaminated by various noise sources or artifacts. These unexpected signals can originate from the electrode-skin interface, in the electronics that are responsible for the amplification, or in the external environment, which may lead to an erroneous

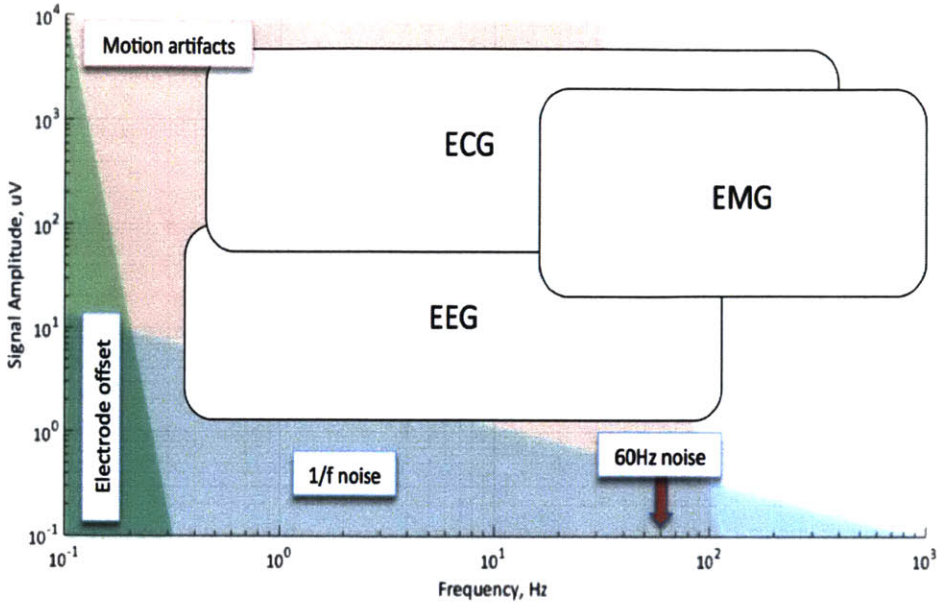

Figure 1-2: Amplitude and frequency characteristics of the biopotential signals [1].

interpretation of the signal. Figure 1-2 shows some of these factors. For example, one of the intrinsic factors is the noise of the system, dominated by the flicker (1/f) noise in the low frequency region. Furthermore, there are external factors such as the electrode interface, the 60Hz power line, the motion-artifacts due to the motion potentials, respiration and so on that interfere with the actual signals. Therefore, the readout circuit design for these systems requires a solid understanding of not only the analog circuit design techniques but also the origin and the characteristics of the signals.

1.1.2 Target Application

The main goal of this thesis project has been to design an ultra-low-power signal acquisition system that will be used for stress monitoring, which is linked to emotional and physical disorders such as depression, frequent headaches, jaw clenching and several other problems.

Recently, some companies have released some stress monitoring products in the

form of wristbands that have shown many different ways of measuring stress levels. One way is to track the electro dermal activity, which measures the electrical characteristics of your skin based on the state of your sweat levels [7]. Another popular physiological marker is the heart rate variability (HRV), where the device detects the intervals between the heart beats [8].

However, in most of these sensors, one of the biggest problems is the personalization required for the sensors themselves. For instance, stress may express itself differently in each individual, i.e., some people may start sweating, while others may get heart palpitations. Hence, it is hard to provide generalized and reliable conclusions that are valid for groups of people.

On the other hand, biopotential signals such as EEG, ECG and EMG have more defined magnitude and frequency characteristics, hence does not require a lot of personalization as the other biomarkers. Taking into account also the fact that tension in the skeletal muscles can provide important diagnostic information about the stress level, we decided to proceed by designing the sensor interface for EMG measurements. Some recent work also used the EMG as a tool to collect diagnostic information for mental stress [9], [10]. We would like to explain two example disorders that are at the focus of the project.

Temporomandibular Joint Disorder

Temporomandibular Joint Disorder (TMJD) is a painful condition in the temporomandibular joint as well as the surrounding muscles and nerves. Common symptoms are pain in the chewing muscles, limited movement in the jaw, difficulty in chewing and headaches. Some of the different treatment ways are applying hot or cold to the muscles to provide relaxation, using bite splints or surgery in extreme cases. Since the symptoms of TMJD can be varied and are complex, it is necessary to find reliable tools before providing diagnostic information to the patients.

Recent studies have suggested that surface EMG (sEMG) measurements can be used for diagnostic [3]. Two good spots in order to take measurements are the temporalis and masseter muscles, which are part of our muscles of mastication. Figure 1-3 shows the location of temporalis and masseter [2]. In order to use surface EMG technique, electrodes are placed on the skin overlying the corresponding muscle to detect the electrical activity.

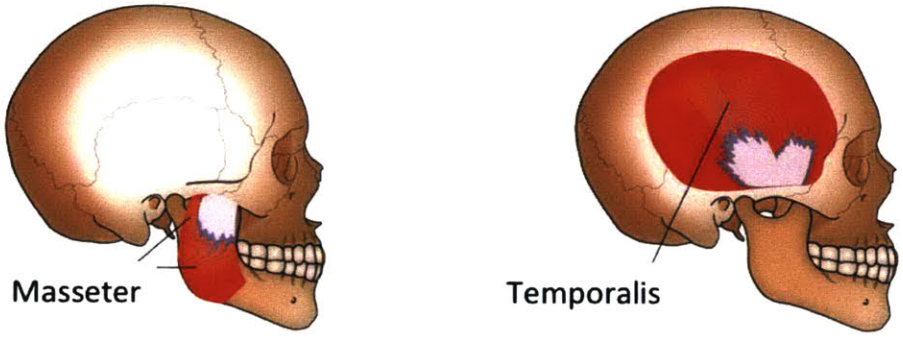

Figure 1-3: Visualization of mastication muscles: masseter and temporalis [2].

In the study presented in [3], the researchers observed that the people with TMJD symptoms exhibit hyperactivity in their mastication muscles compared to the healthy people, i.e., the mean frequency at rest and maximum clenching conditions shift to higher frequencies for the ones with severe TMJD symptoms. In addition to change in frequency characteristics, the strength of the electrical activity was different for the two groups. As Figure 1-4 illustrates, the electrical activity was higher for healthy people compared to the people with TMJD symptoms. In brief, the experiment has shown that the evidence of TMJD can be found both in magnitude and frequency domain for EMG measurements.

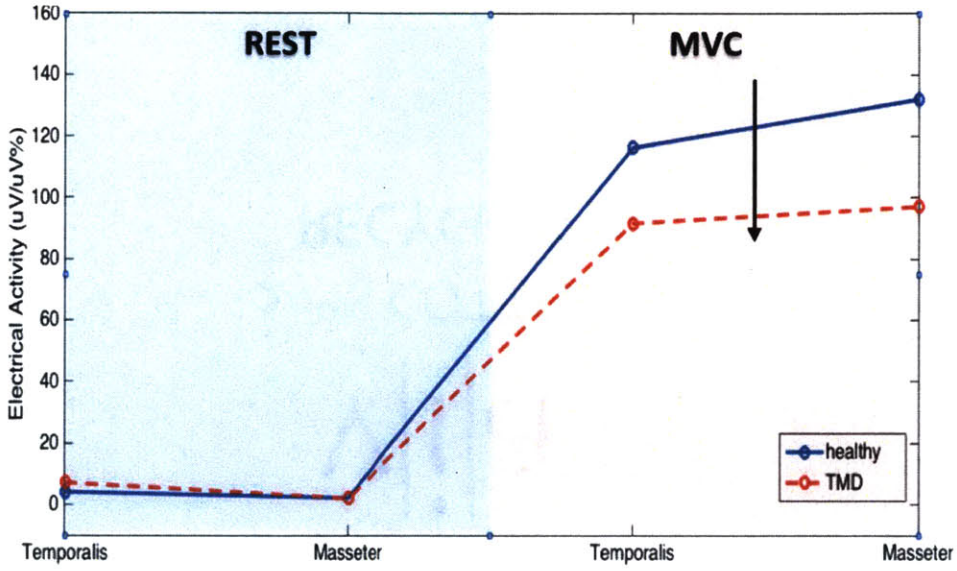

Figure 1-4: Electrical activity of muscles under rest and maximum muscle contraction [3].

Sleep Bruxism

Sleep bruxism is one of the unsolved problems of dentistry, where the patients suffer from teeth grinding and clenching during their sleep. Since TMJD and bruxism disorders have similar signs and symptoms, EMG data is very important in order to get information related to bruxism.

Recently, some commercial devices have been launched, which will allow dentists to objectively collect data to measure bruxism. One of these devices measures jaw EMG signals as well as breathing in order to diagnose bruxism before teeth are damaged [11]. Another device is a low-cost diagnosis-only device stuck to the masseter muscle, while the person is sleeping [12]. At the end of the night, it shows the results of how severe the patient's bruxism was throughout the night as a result of the EMG measurements.

Researchers are also interested in bio-feedback systems that will be able to measure the electrical activity, and stimulate the muscles in order to provide relaxation to these muscles.

1.1.3 Requirements of a Biopotential Acquisition System

Some of the requirements of the biopotential signal acquisition systems can be summarized as follows.

- High common-mode-rejection-ratio (CMRR): The system has to reject the 60Hz line interference, which appears at all the input nodes.
- High-pass-filter (HPF) characteristics: The system should have a certain high-pass cut-off frequency to eliminate the dc electrode offset.
- Low noise: The design should have a low noise floor in order to have high signal-to-noise ratio (SNR).
- Low power consumption: For sensor nodes and implants, the system should dissipate low power for long operation lifetime. Ultra-low power consumption may enable the integration of thin-film batteries, or harvesting the energy from the environment.
- Power-efficiency: The system needs to maintain high power-efficiency, i.e., deliver high performance given their power consumption. Power-efficiency-figure (PEF)

is an important figure of merit showing the power-efficiency of the system.

- High dynamic range: A high dynamic range is desirable as it allows better signal-to-noise-ratio (SNR). The system should tolerate large signal strength variations as well as the large interference signals such as motion artifacts without saturating the system.

- Reliability and robustness: The system should consistently perform the required function under variety of conditions and on the repeated trials.

1.1.4 Current State-of-the-art Amplifier Performances

Table 1.1: Current state-of-the-art low-power biopotential amplifiers

	[13]	[14]	[15]	[16]
Application	ECG	Implantable ECG	Neural	EEG/ECG/EMG
Process (nm)	65	65	65	180
V_{DD} (V)	0.6	0.6	0.45	0.2/0.8
Power (nW)	1	16.8	730	790
Gain (dB)	32	51-96	52	57.8
Bandwidth (dB)	1.5-370	0.5-250	0.25-10000	670
Input noise (uV_{rms})	26	6.52	3.2	0.94
CMRR (dB)	60	55	73	85
PSRR (dB)	63	67	80	80
NEF	2.1	2.64	1.57	2.1
PEF	2.65	4.18	1.2	1.6

1.2 Motivation for Low-Voltage Design

Over the last decade, reducing the power consumption has become the most important priority for the biopotential signal acquisition systems - particularly for the wearable

sensor nodes and implantable devices, since it offers increased battery-life as well as reduces the size and cost of the devices.

In order to have ultra-low-power consumption, both the AFE power and the digital back-end power should be reduced. As we will explore more later in this chapter, biopotential signals fall within sub-kHz range, which makes it relatively easier to scale the digital power. However, the AFE, which consists of the amplifier and the ADC constitutes a bottleneck for the power due to the trade-off between the current drawn in the first stages and the noise of the system [16]. Under these circumstances, it is very attractive to explore low-voltage techniques, which not only enable further power scaling, but also have several other advantages. The remainder of this section will outline the potential benefits of the low-voltage analog design techniques that have motivated our research in this area.

1.2.1 Power Savings

One of the biggest advantages of using low-voltage supplies is to reduce the power consumption of the integrated-circuit (IC). As we are noise-limited in scaling the current levels in the AFE, voltage scaling is a potential alternative to be explored for further power savings.

1.2.2 Minimalist Circuit Topologies

Another benefit of the low-voltage design is that it allows the engineers to reduce the design complexity. Since it is getting trickier to use the conventional topologies with the low supply voltages, researchers are motivated to find alternative topologies as a way to maintain the circuit performance. In the next chapters, we will discuss some of the example work that has been designed using conventional CMOS technology.

1.2.3 Energy Harvesting

Energy harvesting is an important enabling technology necessary to unleash the next shift in mm-scale and μW power computing devices, especially for wireless sensor nodes [17]. For miniaturized, ultra-low power sensing applications, it may be possible to integrate energy harvesting resources to recharge the small batteries that can enable the devices to operate autonomously without the need of changing the batteries. The concept has been shown in a recent work, where they extracted energy from the endocohlear potential (EP) in the inner ear [18]. In the future, this may be used as a biological battery to power several chemical or molecular sensors as well as for drug-delivery actuators for diagnosis and therapy of hearing loss, and other disorders [18].

Comparing the energy available from a $1mm^3$ solid-state thin-film battery [6] with the energy that can be delivered from a $1mm^3$ energy harvester [17], we can see that for a multiyear operation lifetime, it is feasible to benefit from energy harvesting as soon as the power consumption is around singe digit nanowatts. As far as we know, there is only one signal acquisition AFE that has shown power consumption levels in this region [13]. Therefore, it is motivating to investigate alternative approaches in order to achieve similar performance levels.

1.3 Research Goals and Contributions

The main goal of this thesis work is to design an ultra-low power sensor interface for stress monitoring, which can be integrated to wearable and implantable systems for long term signal acquisition. We exploited low-voltage design techniques, which has not been explored much for the analog signal acquisition systems before. In order to scale the system supply, we re-designed the analog architectures by using miniaturized circuit topologies, and using as little cascaded transistors as possible in the stages in

order to guarantee proper sub-threshold transistor operation. As a result, we achieved sub-nW power consumption in the amplifier, and 4.1nW power consumption in the overall system with a power-efficiency-factor (PEF) of 1.57, while ensuring enough gain, linearity and reliability.

We can see from the recently published low-power biopotential amplifiers that are presented in Table 1.1 that it is challenging to present both ultra-low power and very low PEF at the same time due to the increase in the noise level with decreased current consumption in the system. By leveraging low-voltage design, our work manages to overcome this trade-off, and achieves both very low power consumption and very low PEF at the same time. Also, we ensure high closed-loop gain in the AFE, which reduces the required number of bits in the digitization, and relaxes the ADC design requirements. In addition to these, we provide a motion-artifact cancellation capability in the system that suppresses the undesired environmental interference signals from amplification.

We believe that the simplistic design techniques that we explored in this project can be further improved, and be integrated with low voltage DSP blocks in order to design miniaturized sensor nodes.

1.4 Thesis Organization

The thesis is organized as follows. In Chapter 2, we will investigate the challenges in low-voltage low-power (LV-LP) analog design. We will look into the the technologies that have recently been used for LV-LP analog design, specifically concentrating on CMOS technology. We will derive equations, and calculate the theoretical limits for important amplifier parameters. After emphasizing the challenges in designing LV-LP AFE systems, we will continue in Chapter 3 by explaining the AFE architecture and the conceptual design of the system. We will provide a system overview including

the important design considerations coming from the application as well as from the sub-blocks. In Chapter 4, we will give the circuit design details mostly for the amplifier and the amplifier-ADC interface. After that, we will show the simulation results for the extracted AFE. At the end of this chapter, we will compare our performance with the state-of-the-art work that have been published recently. Finally, Chapter 6 will be the conclusion, where we will emphasize on our contributions, and briefly discuss the future work.

Chapter 2

Challenges in Low-Voltage Low-Power CMOS Analog Design

Complementary metal oxide semiconductor (CMOS) technology is the most conventional, less expensive and the most robust technology that has been used for transistor fabrication. In the recent years, as the technology nodes make it possible to fabricate smaller devices, several trade-offs show themselves in the performance of devices. In this chapter, we will give an overview on the challenges in low-voltage low-power (LV-LP) CMOS analog design. While discussing the challenges, we will derive the equations for the important amplifier metrics that we will use in the following chapters.

2.1 Sub-threshold Circuit Operation

As the technology nodes keep following the Moore's law, the transistor sizes are getting smaller. As the dimensions of the devices shrink, the supply voltage should scale down accordingly in order to maintain the device reliability. However, the threshold voltage is not scaled down by the same ratio, since devices with higher threshold voltage value have higher noise margin and smaller leakages [22].

For the case of LV-LP applications, the transistors usually operate in sub-threshold

regime to save power. However, in order to meet the noise and the dynamic range requirements, certain amount of current should flow through the transistors, which exponentially depends on the threshold value. Hence, it is challenging to use low-voltage supplies and provide enough overdrive voltage for the transistors to have reasonable current levels.

2.2 Device Noise

For LV-VP applications, in order to maintain a desired dynamic range under a scaled supply voltage, the noise power in the circuit must be scaled proportionately, which requires increase in the current consumption for purely noise-limited designs [24]. This constitutes a bottleneck to the power consumption. In order to address this challenge, it is important to be aware of all the noise sources external and internal to the system.

Cable interface, the motion potentials and respiration are some examples of external noise sources, which are possible to deal with by using different techniques that are available in modern electronics. On the other hand, the intrinsic noise sources such as the thermal noise and the flicker noise originate from the devices, and bring a limitation to the minimum current consumption to the system based on the application requirements.

2.2.1 Shot Noise

The shot noise is caused as a result of the current flowing through the transistor channel not being smooth. For sub-threshold regime, the shot noise current source can be modelled by using Equation 2.1 [25].

$$\overline{\Delta I_n{}^2} = 2qI_{DSAT}(1 + e^{-V_{DS}/\phi_t})\Delta f \tag{2.1}$$

where ϕ_T is the thermal voltage,which is around 26mV at room temperature, Δf

is the noise bandwidth and I_{DSAT} is the saturation current given by Equation 2.2.

$$I_{DSAT} = I_{OS} e^{\kappa V_{GS}/\phi_t} \tag{2.2}$$

$$I_{OS} = \mu C_{OX} \phi_t \frac{W}{L} \left(\frac{1-\kappa}{\kappa} \right) e^{-\kappa V_T/\phi_t} \tag{2.3}$$

where I_{OS} is a process and transistor dependent constant. As seen from Equation 2.3, its value is set by the parameters such as the mobility(μ), the oxide capacitance (C_{OX}), the width(W) and length(L) of the transistor, the gate coupling coefficient(κ), the threshold voltage(V_T) and ϕ_T. Note that the value of κ for recent technologies is around 0.7-0.8.

In the calculations, we will use the input-referred shot noise expression for convenience. In order to model the shot noise as a voltage source at the input, we need to divide Equation 2.1 by the transconductance. In sub-threshold saturation, the trasconductance and current are related through Equation 2.4.

$$g_m = \frac{\kappa I}{\phi_t} \tag{2.4}$$

Using Equation 2.4, we can obtain the input-referred voltage noise as follows.

$$\overline{\Delta V_n{}^2} = 2\frac{g_m k T \Delta f}{\kappa} \simeq \frac{8}{3 g_m} k T \Delta f \tag{2.5}$$

We will use Equation 2.5 in the derivations of the input-referred noise of the design in Chapter 4.

2.2.2 Flicker (1/f) Noise

Flicker noise is a significant source of noise in MOS devices. It is also called as $1/f$ noise since the spectrum varies as $1/f^{\alpha}$, where α is very close to unity. Even though

the origin of the flicker noise is not very well defined, the noise voltage source can be modeled by using Equation 2.6.

$$\overline{V_n^2} = \frac{K}{WLC_{OX}f} \tag{2.6}$$

where K is a process parameter that depends on W and L. We should note that $1/f$ noise dominates the frequency spectrum for low frequencies, and the frequency at which the $1/f$ noise is equal to the shot noise is called the $1/f$ corner frequency f_c.

Especially for EEG and ECG applications, the elimination of $1/f$ noise is crucial since a lot of information about the signal lies in this region. Chopper-stabilization amplifiers are commonly used in order to remove the effect of $1/f$ noise [26]. In this technique, the desired signal is shifted to higher frequency bands, and the $1/f$ noise is removed by using a high-pass-filter (HPF). Once the noise is removed, the signal is shifted back to its original spectrum. We should note that, chopping requires extra power, which results in additional power consumption in the amplifier. However, for our target application, EMG, the effect of $1/f$ is much less compared to EEG and ECG. Therefore, it is be possible to shift f_c to $20Hz$ range by sizing up the input transistors, and use the amplifier without any chopper-stabilization.

2.3 Noise/Power Efficiency

In low power signal acquisition systems, the power dissipation is dictated by the tolerable input-referred thermal noise of the amplifier, where the trade-off is expressed in terms of noise-efficiency-factor(NEF) [27]. Similarly, PEF is the measure of how efficient the system is for a given power consumption. Conventional systems face limitations in achieving good NEF/PEF and low power consumption at the same time.

Equation 2.7 shows the expression for the NEF.

$$NEF = V_{in,rms}\sqrt{\frac{2I}{\pi \cdot \phi_t \cdot 4kT \cdot BW}} \tag{2.7}$$

where $V_{in,rms}$ is the input referred rms noise, I is the total supply current, k is the Boltzmann constant and BW is the bandwidth of the amplifier.

At this point, it would be interesting to find the theoretical minimum of NEF for a differential OTA with two input transistors, two load transistors and a tail current source. We will only take into account the input and the load transistors as the noise contributors. Ignoring the effect of the flicker noise, and assuming $I = 2I_{ds}$, we can derive the theoretical minimum for the NEF as in Equation 2.8.

$$NEF \simeq \overline{V_n}\sqrt{BW}\sqrt{\frac{2}{\pi \cdot \phi_t \cdot 4kT \cdot BW} \cdot \frac{2g_m\phi_t}{\kappa}} \tag{2.8}$$

Putting Equation 2.5 into Equation 2.8 and using $\kappa = 0.85$ we can find the theoretical limit to be $\sim$2.

Similarly, PEF is defined from NEF by using the following equation.

$$PEF = NEF^2 \cdot VDD \tag{2.9}$$

By using the theoretical limit for the NEF, the theoretical PEF for a supply voltage of 0.3V can be found as 1.2.

2.4 Distortion

In the AFE, it is ideal to have a linear amplification, i.e. when the input is increased by a certain percent, the output should increase by the same percent. However, as the small signal amplitudes increase, the output starts suffering from distortion due to nonlinearity in the amplification. In order to improve the linearity of the amplification, closed-loop amplifiers with high open-loop gain are preferred. This is because of the

fact that by exploiting feedback, the closed-loop gain is set to a desired value, which is independent of the nonlinearity in the open-loop gain as soon as the loop-gain is high.

However, as the signal levels increase, the transistors at the amplification stages go out of saturation regime, which results in drop in the open-loop gain. Hence, distortion occurs at the output. The distortion becomes more of a problem for low-voltage designs, since it is harder to keep the transistors in saturation regime, and have a high loop gain.

2.5 Dynamic Range

Dynamic range, usually measured in dB, is the ratio of the maximum and minimum useful signals at the amplification. The minimum useful signal is determined by the noise level, and can be expressed in terms of the total input-referred peak-to-peak noise. On the other hand, the maximum useful signal is proportional to the V_{DD}, and limited by the distortion. The total-harmonic-distortion (THD) is a good measure of the distortion in the system, which is the ratio of power of all the harmonic components at the output to the power of the fundamental signal frequency. Equation 2.10 shows the definition of THD. The maximum allowable THD is determined by the application, which determines the maximum useful signal at the output for dynamic range calculations.

$$THD = \frac{\sqrt{{V_2}^2 + {V_3}^2 + {V_4}^2} + \cdots}{V_1} \tag{2.10}$$

In addition to all these constraints, the systems should have a headroom for large signals such as the motion artifacts, which puts an additional limitation to the system dynamic range. The signal swing at the output should allow large signals without saturating the AFE. Hence, it is very challenging to maintain reasonable dynamic range values in LV-LP applications.

2.6 Summary

In this chapter, we discussed the popular technologies used for LV-LP analog design. We investigated the challenges for CMOS analog circuit design, since it has been the most commonly used technology for the past decades. We derived the necessary equations and theoretical limits for certain parameters, which will be important to compare with our design.

Chapter 3

AFE Architecture

This chapter will describe the proposed AFE architecture without going into the circuit details of each block. In Section 3.1, high-level system requirements and design issues that affect the system architecture will be presented. In Section 3.2 and Section 3.3, block-level design considerations for the amplifier and the ADC will be discussed, respectively. More detailed analysis of the system will be provided in Chapter 4.

3.1 System Level

This section will discuss the system level design requirements of the AFE determined by the project goals as well as by the target application.

3.1.1 Required Gain and Resolution

In the proposed AFE, the amplifier should provide enough amplification, and the ADC should digitize the analog signal with enough resolution. In doing that, it is important to select the optimal values for the design parameters such as the gain, the V_{DD} and the number of ADC bits according to the application of interest.

For EMG signals, the peak-to-peak signal levels may change between 20μV - $2mV$

as shown in Figure 1-2. Hence, for proper operation, the amplifier should be able to amplify any signal between this range, and the ADC should have enough resolution in order to be able to digitize signals as small as $20\mu V_{pp}$. Considering fully differential operation, the input referred resolution can be found by using Equation 3.1.

$$Resolution = \frac{2 \cdot V_{DD}}{2^N} \tag{3.1}$$

where N is the number of ADC bits. Note that the supply voltage is determined by the dynamic range requirement of the AFE. The selection of V_{DD} puts the constraint on the maximum achievable resolution of at the ADC.

Table 3.1 shows the resolution of the fully differential AFE for a given V_{DD}, number of ADC bits and the gain value. In order to have a resolution around $20\mu V$, and to scale down the supply voltage, we chose the parameters that are in the highlighted row as our design specs. We could have increased the resolution even more, as it is shown in the third row, by utilizing a 10 bit ADC, but this would increase the ADC area as well as would make the design more complicated. Hence, we set the ADC bits to be 8, which required to have a closed-loop gain of 100 at the amplifier side. This is a reasonable value to satisfy with 3 stage design.

Table 3.1: Input resolution for different V_{DD}, number of ADC bits and gain values.

Resolution (μW)	VDD (V)	ADC Bits	Gain (dB)
23	0.6	10	50
46	0.6	8	100
11	0.3	10	50
23	**0.3**	**8**	**100**

3.1.2 Motion Artifact Cancellation

Motion artifacts are interference signals that interfere with the biopotential signals during the measurements. Electrode/cable interface, motion potentials, eye blinking and respiration are examples of motion artifact signals. Since they are usually larger signals than the actual signal of interest, they may saturate the AFE. Hence, it is required to have sufficient dynamic range in order to tolerate these large interference signals without saturating the system.

In the frequency domain, these noise sources have frequency spectra that contaminate the low-frequency region of the EMG spectrum. Figure 3-1 shows the frequency spectrum of the artifact signals together with the actual EMG spectrum [4]. As seen, there is a low-frequency region, where both the real EMG signals and the motion artifacts signals exist together. Hence, it is non-trivial to remove the motion artifacts and preserve the desired information without any compromise.

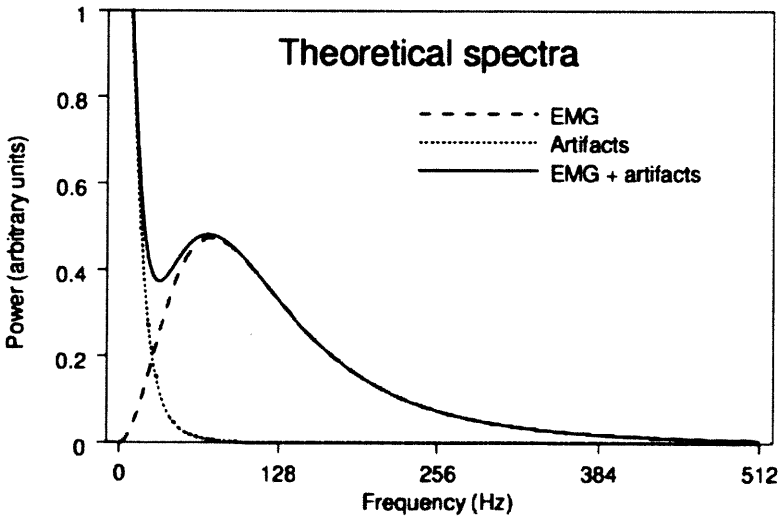

Figure 3-1: Representation of artifacts and EMG in frequency domain [4].

One of the reference studies in this area suggests to use a butterworth filter with a corner frequency of $20Hz$ and a slope of $12dB/oct$ for optimal sEMG measurements [29]. However, even with the cut-off around $20Hz$, we would still observe the effect of

the motion artifacts at the output of the system. Since shifting the high-pass cut-off to even higher frequencies would cause information loss, it is important to explore other ways of canceling the remaining large signals from the system.

Numerous methods have been presented in the literature in order the cancel the effects of the motion artifact signals. Some of the examples to the offline cancellation methods, where the cancellation is achieved after the signal acquisition are adaptive filtering [30], wavelet transforms [31] and computational methods such as Independent Component Analysis (ICA) and Principal Component Analysis (PCA) [30]. In adaptive filtering, a reference signal such as the electrode-skin impedance must be used in order to track the noise generated by the motion artifacts, and to adjust the parameters of the adaptive filter [30]. However, introducing an additional reference signal to the system increases the design complexity. On the other hand for ICA/PCA techniques, the noise and the actual signal of interest are in general assumed to be linearly independent, which brings a limitation to the conclusions made by these algorithms. However, the offline cancellation techniques does not relax the ADC requirements, and may cause the system to saturate under the presence of the motion artifacts. In contrast, if the cancellation is achieved in the analog domain, the amplifier can be used without being saturated, reducing the system dynamic range requirement. An example of real time cancellation was presented in [32], where the focus was to cancel the dc offset of the dc-coupled neural signal acquisition system. Mixed-signal feedback techniques were used in order to mitigate the offset with a fixed transfer function in the feedback loop. In this way, not only the dc offset but also the low frequency artifact components were filtered from the output.

Therefore, in this work, we propose a mixed-signal artifact cancellation loop, which manages to cancel the low frequency artifact signals in real-time, without affecting the signals in the main frequency band. Figure 3-2 shows a representation of the idea.

In the figure, the blue signal represents the actual EMG signal that is recorded,

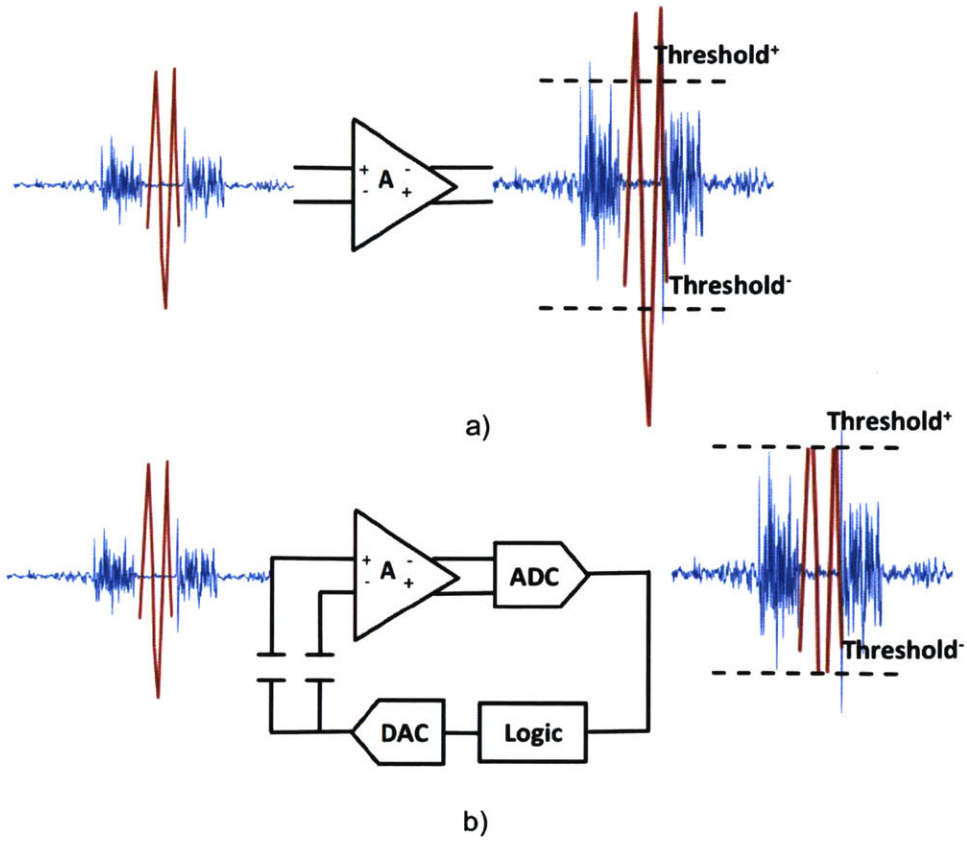

Figure 3-2: Conceptual idea of cancelling motion artifacts.

and the red signal represents the undesired motion artifact on top of it. If the system does not have any mechanism to reject these artifacts, these signals would both get amplified, and the system would saturate because of the presence of the large signal. In our proposed motion artifact cancellation scheme, we first detect the presence of the artifact. Once we decide that the artifact is present, we send the information to a logic, which decides the amount of the signal that needs to be subtracted from the input in order to keep the signal levels between the thresholds. Finally, the DAC converts the output code of the logic block to an analog step, and feeds it back to the input for subtraction. By subtracting/adding steps, the loop prevents the system from saturation in the presence of the motion artifacts. We should note that the purpose of the proposed scheme is to not to saturate the amplifier during the operation. Since the motion artifact signals are effective in a frequency band of 0-20Hz, the steps

added/subtracted from the output will not hurt the actual EMG signal, while keeping the overall amplification between the thresholds. The detailed circuit design of the motion artifact cancellation block will be presented in Chapter 4.

3.1.3 Minimum Required Current

Since one of the main goals in this project is to push the limits of the power consumption in the AFE, it is necessary to put the limit on the minimum input current required for reliable amplification. In this respect, the minimum required input current is set by the maximum allowable noise floor in the application, which is related to the minimum expected signal levels in the frequency domain. In a previous single-digit-nW signal acquisition AFE [13], reliable ECG information has been extracted by having a current of $\sim 1nA$ in each branch of the first stage amplifiers. Since the signal of interest in our design is EMG, which has higher magnitudes relative to ECG signals as shown in Figure 1-2, we found it reasonable to have a current consumption of $1nA$ in each branch at the first stage. Allocating negligible current to the following stages, the total current flowing through the closed-loop amplifier was kept $\sim 3nA$ to save power.

3.2 Amplifier

This section will describe the conceptual idea behind the proposed amplifier design. We will first investigate one of the most classical operational transconductance amplifier (OTA) topologies in order to identify its limitations for LV-LP design. After introducing the proposed inverter-based topology, we will discuss one of its biggest potential problems. Then, we will continue with some approaches that have been published to address this problem. Finally, we will explain our design solution.

3.2.1 Inverter-based Topology

Figure 3-3 shows one of the most conventional OTA topologies that have been used by the designers for many years, where M_0 behaves as the current source, M_1-M_2 are the input transistors, and M_3-M_4 are the load transistors. In this topology, M_0 not only provides the constant current supply, but also is very important for common-mode rejection. We can explain this situation by looking at the small signal analysis of the OTA.

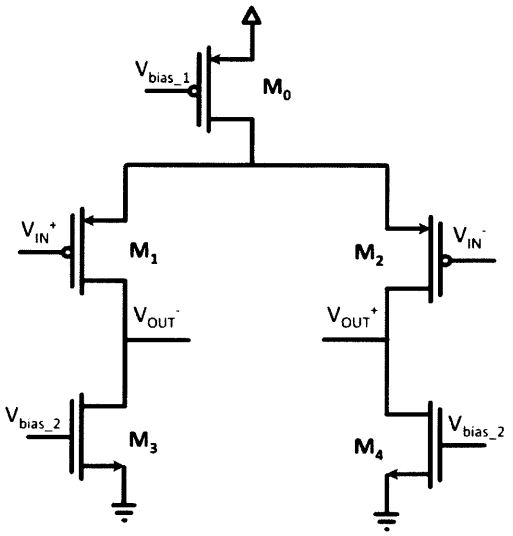

Figure 3-3: Classic 5-transistor OTA topology.

When the input is differential, the drain of M_0 acts as a virtual ground. The single-ended gain of the amplifier can be found by multiplying the g_m of the input transistors with the equivalent output resistance at the output node. On the other hand, when both inputs are the same, only a small fraction of the input is amplified due to the voltage division between the V_{ds} of M_0 and the V_{gs} of the input transistors. Hence, the simple 5-transistor topology can provide high gain for differential signals, and can provide sufficient common-mode rejection. Therefore, it has been used in the signal acquisition systems for many years.

However, this conventional OTA topology brings limitations to the amplifier, when

the voltage supply is very low. This is due to the fact that the topology has 3 stacked transistors in each branch, and each of them requires $\sim 100mV$ drain-to-source voltage in order to stay in sub-threshold saturation regime. Furthermore, it needs to provide enough swing at the output node for amplification. For instance, for an application, where we choose the supply voltage to be $0.3V$, the amplifier would suffer from nonlinearity, since the transistors would no longer be in the correct regime for amplification.

The problem of not being able to satisfy the sub-threshold saturation condition because of having many cascaded transistors in each branch motivated us to simplify the topology even further. As a result, we decided to remove the tail transistor, and use only two cascaded transistors, which is called as the pseudo-differential topology. Figure 3-4 shows the pseudo-differential circuit that we made use of in the design of our core amplifier.

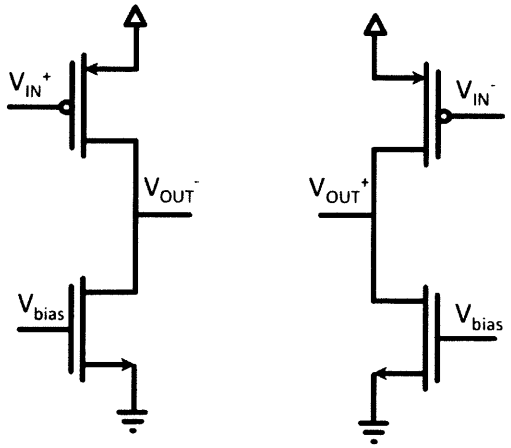

Figure 3-4: The illustration of the simple pseudo-differential amplifier structure.

Now that we removed the tail transistor, we can provide more voltage headroom for the two transistors. Hence, even with the $0.3V$ supply, we can make sure that the sub-threshold saturation condition will be satisfied with enough swing at the output node. The details of the circuit will be discussed in Chapter 4.

3.2.2 CMFB Problem

By removing the tail transistor from the 5-transistor OTA, we lose the mechanism that rejects the common-mode signals. Hence, the new amplifier will treat both the differential-mode signals and the common-mode signals in the same way and amplify them. As a result, the CMRR is equal to 1.

This means that any common-mode signal at the input such as the $60Hz$ line interference signal will propagate to the output by getting amplified. Since these undesired common-mode signals can have large magnitudes, this may saturate the amplifier.

The CMRR problem can be solved by integrating a supporting common-mode-feedback (CMFB) block to the system. In the recent years, there has been some alternative work that have explored the inverter-based pseudo-differential topology and the integration of different CMFB blocks [33], [34]. In both of these designs, the bulk terminal of the input PMOS transistors were used in order to feed the amplified common-mode signal back to the circuit. Since the bulk transconductance, g_{mb}, is much smaller than the gate transconductance, g_m; feeding the amplified common-mode signal to the bulk leads to lower CMRR compared to feeding it to the gate of the load transistor. For example, in [33], the resultant CMRR was -15dB, where as the exact value of the CMRR in [34] is not known.

In our design, we preferred to use the gate of the load transistor as the feedback node in order to increase the common-mode rejection in the design. Figure 3-5 shows the block diagram representation of the CMFB block, when it is connected to the pseudo structure. The purpose of that block is to sense and suppress the signal, whenever it is a common-mode signal. When it is active, it amplifies the common-mode signals, and feeds the amplified output to the gate of the load transistors in negative feedback configuration. Eventually, the common-signal gets suppressed at the output of the amplifier.

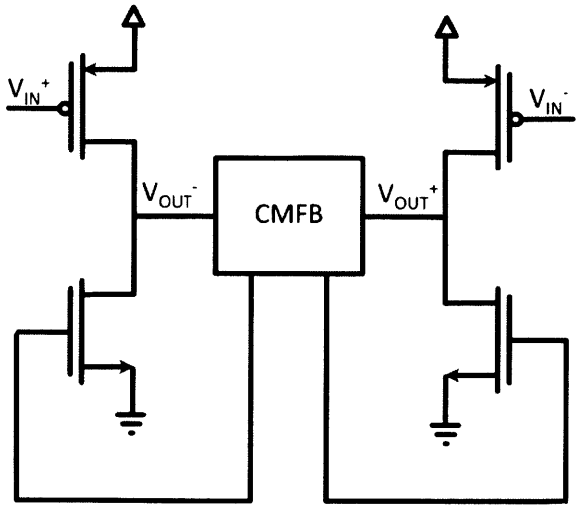

Figure 3-5: Proposed CMFB Architecture.

The feedback block diagram representation is given in Figure 3-6. As it is seen from the figure, for the common-mode signals, the CMFB block provides a negative feedback to the input of the amplifier, and prevents the signals from being amplified. However, for the differential signals, the CMFB block acts as an open circuit, and the stage amplifies the signals as desired. The analysis of the circuit will be provided in Chapter 4.

3.3 ADC

The other component of the designed AFE is the ADC, which is responsible for digitizing the analog data coming from the amplifier output. The ADC that is presented in this work was designed by Harneet Singh Khurana. In this section, without going into the details, we will discuss the important design requirements of the ADC.

As we have mentioned in the system requirements, in order to provide enough resolution, a 8 bit successive approximation ADC (SAR ADC) was designed. In addition to providing 8 bit resolution, there were several other constraints on the

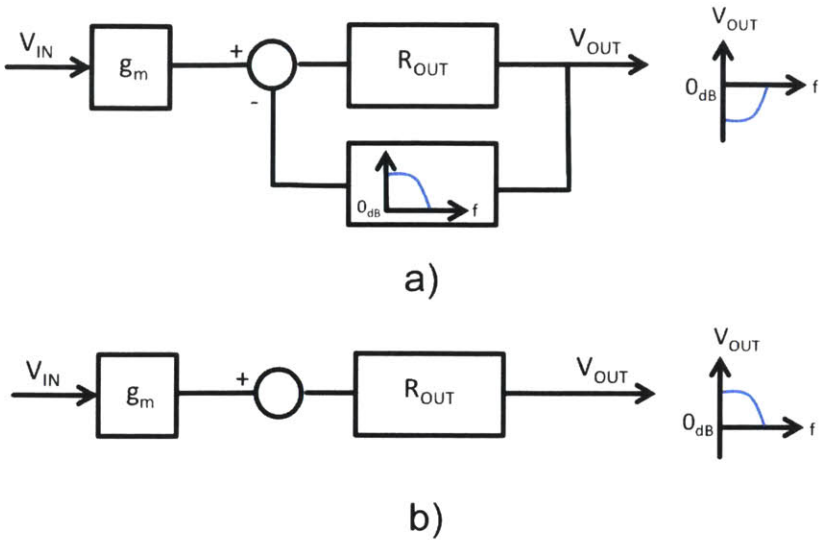

Figure 3-6: Block diagram representation of the CMFB idea. a) The block diagram of the amplifier stage for the common-mode signal. b) for differential-mode signals.

ADC.

One of the constraints was to work with $0.3V$ power supply, which was chosen to be the system power supply. When the ADC operates from such low supply with 8 bit resolution, the least-significant-bit (LSB) size becomes very small. This brings a limitation to the minimum current that the input comparator can have in order to reduce the noise of the comparator. Otherwise, it would not be possible to ensure enough resolution because of the noise. Hence, a dynamic comparator was designed and it was sized to reduce noise below 1 LSB of the ADC, which was around $2.3mV$.

In addition, according to the Nyquist criteria, the ADC should have a clock, which should be at least two times higher than the highest input frequency to prevent frequency aliasing. Considering the fact that the low-pass cut-off frequency of the amplifier was chosen to be $\sim 450Hz$, the ADC clock was set to $1kHz$. Hence, the sample rate was $1kS/s$.

Another requirement that the ADC should satisfy was to have as small sampling capacitance as possible. This was due to the fact that the amplifier was interfaced

with the sampling block of the ADC, which was reset at every millisecond. Hence, the amplifier should charge the sampling capacitance of the ADC after each clock cycle. If the ADC could provide smaller capacitance, then less current would be required for charging. For this purpose, split digital-to-analog-converter (DAC) architecture was chosen to separate out the sampling capacitance by sampling the input only on the main DAC, while using the full DAC during the conversion. The details of the split DAC ADC architecture is well explained in a recent work, where they presented a reconfigurable and voltage scalable ADC [35]. Using the split DAC architecture in the ADC, we decreased the overall capacitance compared to a binary-weighted DAC, and provided area savings. Figure 3-7 shows the split-DAC ADC structure used in our design.

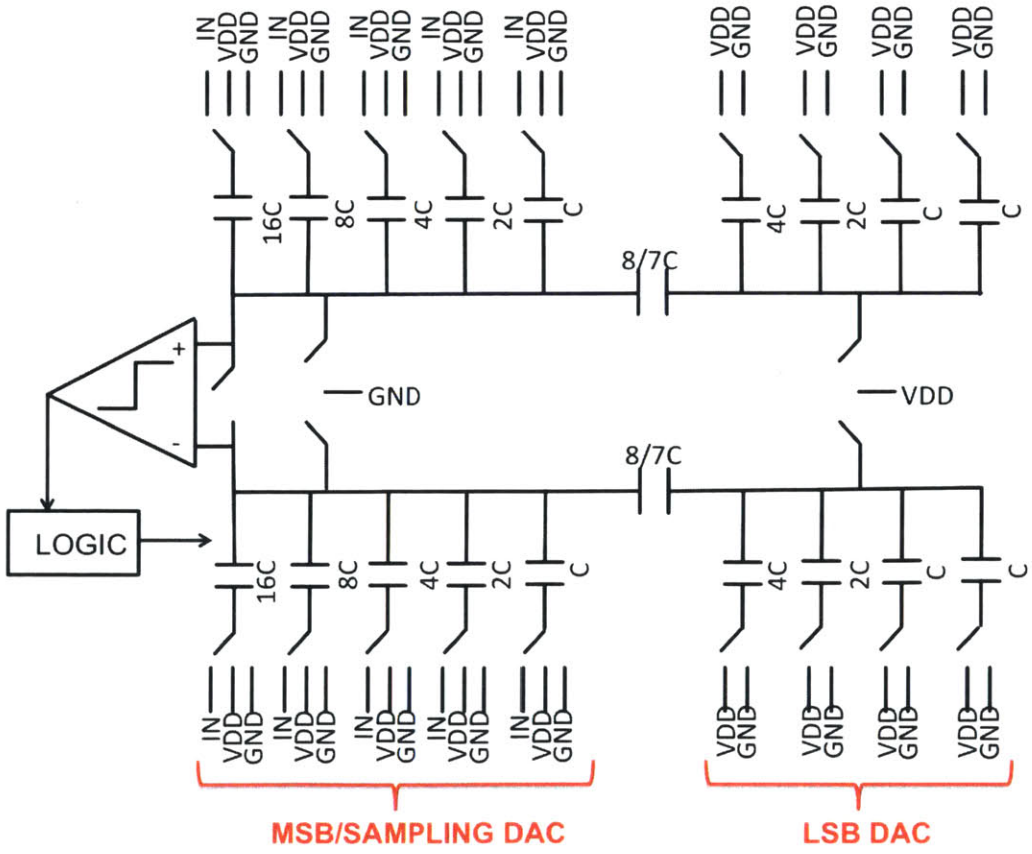

Figure 3-7: Split-DAC, fully differential ADC.

The performance of the ADC will be provided in the Chapter 4, where we will present the simulation results.

3.4 Summary

In this chapter, we discussed the AFE architecture and the design requirements. We started with the system level requirements and the design issues that have affected the system architecture.We explained the idea behind the amplifier design by comparing it with the recently published amplifiers, which used similar pseudo-differential topology. Finally, we briefly introduced the ADC, which was designed by Harneet Singh Khurana. In Chapter 4, we will go into the circuit design details of each of these blocks, and derive the analytical expressions for the important design parameters.

Chapter 4

Circuit Design Details

In this chapter, we will discuss the details of the circuit design of the AFE that is shown in Figure 4-1.

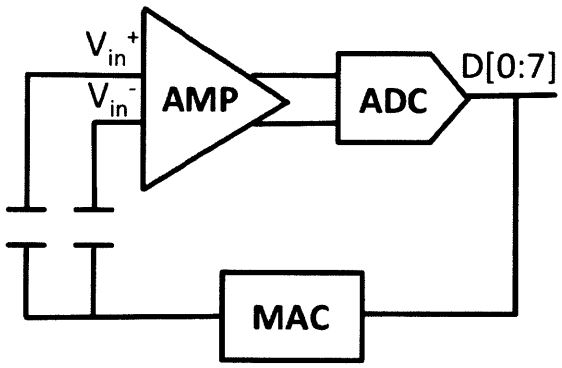

Figure 4-1: System description.

The AFE consists of an amplifier, an ADC, and a motion-artifact-cancellation (MAC) block. The system takes the input from two channels, and after the amplification and the digitization steps, provides a 8 bit digital output. The MAC loop, which is responsible for the suppression of the undesired large signals, is integrated into the system in the feedback loop.

In Section 4.1, we will start with the amplifier circuit design. In section 4.2, we will investigate the implementation of the MAC block, and show its integration to the

system. In Section 4.3, we will look into the system level block diagram, and explain the design of the ADC together with the interface and output buffers. Finally, we will summarize the chapter.

4.1 Amplifier

In this section, we will analyze the amplifier by showing the schematics of each block. We will start by the analyses of the main amplifier. Then, we will continue with the explanation of the reference voltage generation and the resistor implementation. Finally, we will show the closed-loop amplifier structure together with the feedback elements.

4.1.1 1^{st} Stage

In Section 3.2, we discussed the conceptual design of the amplifier stage. We emphasized the importance of creating a support block, which is responsible for rejecting the common-mode signals. In this section, we will investigate the amplifier stage in detail by analyzing its behavior for differential-mode an common-mode signals. We will see that the CMFB block operates when the input signals are common, and becomes an open circuit when the signal is in differential-mode. The schematics of the amplifier stage together with the CMFB circuit is shown in Figure 4-2.

In this circuit, M_1 and M_2 are the input transistors, while M_3 and M_4 are the load transistors of the amplification stage. The resistors denoted as R_P are used as common-mode sensors. Whenever the output nodes are differential, node V_C becomes a virtual ground. On the other hand, for common-mode output signals, the resistors act as a common-mode sensor, and the sensed signal is sent to the CMFB block through node V_C. The CMFB block consists of two stages in order to provide odd number of total amplification for the common-mode signals. This is necessary in

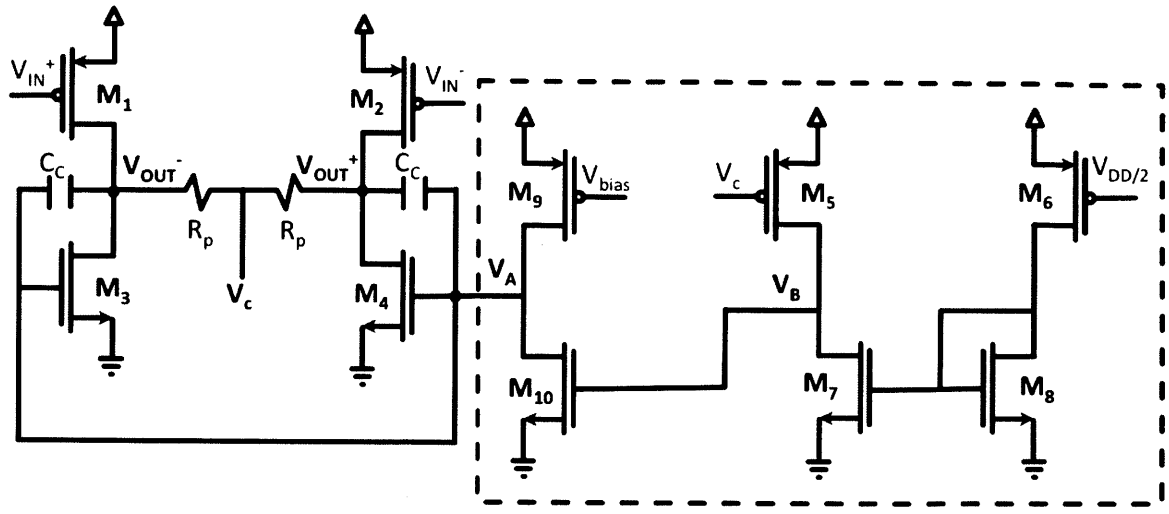

Figure 4-2: First stage.

order to ensure the negative feedback. In addition to the common-mode rejection, the CMFB is also responsible for setting the dc value at the output nodes to $V_{DD}/2$. This is achieved by setting one of the inputs to a reference voltage of $V_{DD}/2$, and providing high open-loop gain in the CMFB loop. Finally, the compensation capacitors C_C are used in order to make the common-mode circuit stable. As we will see in the analysis, they play important role in determining the frequency response of the amplifier. Note that, we will refer to the notations in Figure 4-2, while doing the differential-mode and the common-mode differential-mode analysis.

Differential-Mode Analysis

The circuit can be simplified when the input signals are differential. First of all, for differential signals, the common-mode sensing node V_C becomes a virtual ground, which puts R_P in parallel with the output resistance of the amplifier. Second simplification comes from the fact that node V_A also acts as a virtual ground due to the symmetry in the circuit. As a result, the CMFB block does not have any effect on the amplification for the differential-mode signals. In the simplified small signal circuit, we can find the differential gain by multiplying the transconductance of the input transistors with the

equivalent load at the output nodes. The approximate transfer function for the first stage differential gain, $A_{1,diff}$, can be written by using the following equations.

$$A_{1,diff} \simeq \frac{A_1}{1 + s/\omega_1} \tag{4.1}$$

$$A_1 = -g_{m_1} R_{out_1} \tag{4.2}$$

$$R_{out_1} = R_{1,2}//R_{3,4}//R_P \tag{4.3}$$

$$\omega_1 \simeq \frac{1}{R_{out_1}(C_C + C_L)} \tag{4.4}$$

Note that the value of R_P in the design was chosen to be much higher than the output resistances of the gain transistors in order not to affect the differential gain. Furthermore, C_L in Equation 4.4 represents the load capacitor of the first stage, which is the input capacitor introduced by the second stage.

As we have discussed in Section 3.1.3, the current flowing through the branches of the first stage amplifier is $\sim 1nA$, which is much larger than the current levels at the following stages. Intuitively, this motivates us to make that pole a non-dominant pole due to the relatively small output resistance available at the first stage. By choosing the value of the C_C accordingly, we shifted ω_1 to higher frequencies. We will discuss the numerical values for these expressions further in this chapter, while discussing the stability of the amplifier.

Common-Mode Analysis

The CMFB block cannot be considered as an open circuit for the common-mode signals. In this case, node V_C detects the output common-mode, and the CMFB

block amplifies, and feeds it back to the amplifier. The CMFB block is connected in negative feedback configuration as we have seen in Figure 4-2. Compared to the differential-mode analysis, the common-mode analysis is more complicated, since the circuit cannot be simplified as in the differential case.

However, the gain expression can easily be calculated by using the feedback block diagram in Figure 3-6. In the feedback path of this diagram, the gain block represents the amplification in the CMFB circuit. If we define the gain from the node V_C -> V_B as A_B, and the gain from the node V_B -> V_A as A_A, we can represent the feedback transfer function as $-g_{m_3}A_BA_A$. This shows the current that is fed back to the amplifier by the CMFB block as a result of the two stage amplification of the output signal. Treating C_C as an open circuit for low frequencies, the common-mode gain, $A_{1,com}$, can be found as follows.

$$A_{1,com} \simeq \frac{A_1}{1 + g_m R_{out_1} A_A A_B} \tag{4.5}$$

where g_m refers to the transconductance of M_3. From now on, we will simply use g_m to represent the transconductances of M_1, M_2, M_3 and M_4, since their values are very close to each other. In this equation, the important thing to note is that the low frequency gain of the transfer function is $\sim 1/A_AA_B$. On the other hand, the dominant pole in the CMFB circuit comes from node V_A, due to the large capacitor C_C at that node, which causes a voltage division between the output node and V_A for higher frequencies. This pole appears as a dominant zero in the closed-loop common-mode circuit representation, and is important in determining the bandwidth of the common-mode transfer function of each stage. The approximate location of this pole can be written as in Equation 4.6.

$$\omega_1 \simeq \frac{1}{R_9 // R_{10}(2C_{gs_3} + 2C_C)} \tag{4.6}$$

The numerical values for the related parameters will be provided together with the values for the gain stages. We should note that the most important consideration in choosing the location of the dominant poles in the common-mode analysis is to locate them such that the circuit provides enough suppression for $60Hz$ interference signals, by keeping in mind that the closed-loop configuration does not affect the location of the open-loop poles for the common-mode analysis due to the very small forward gain. The details of this statement will be presented in the closed-loop amplifier discussion.

Noise

The input-referred noise can be calculated by taking into account the noise coming from all the stages. While doing that, the noise of each stage should be divided by the gain until that stage in order to transfer its noise to the input. As a result, the stages following the first stage add negligible amount of noise to the system as long as the gain of each stage is high enough. On the other hand, the noise of the first stage dominates the noise, since it directly appears at the input of the amplification. At this point, it is useful to calculate the input noise voltage of the amplifier by taking into account only the first stage noise.

In the schematics of the first stage as shown in Figure 4-2, there are four transistors (M_1, M_2, M_3 and M_4) that dominate the noise. In addition to these transistors, there are other noise sources such as the R_P as well as the CMFB transistors. However, as soon as the resistors are well-matched, the noise coming from these resistors can be ignored. In order to increase the matching, common-centroid techniques can be utilized in the layout of the pseudo-resistor implementation. Furthermore, the noise of the CMFB block is not added to the output noise, since it appears at the input of both stages.

Taking into account only the four transistors at the first stage, and considering only the thermal noise, we can find the total input-referred noise density by using

Equation 2.5.

$$\overline{V_{n_{total}}^2} = 4 \cdot \frac{8}{3} \frac{kT}{g_m} \tag{4.7}$$

Using Equation 2.4 with $I = 1nA$ and $\kappa = 0.85$, the g_m can be found as $33nA/V$. Hence, the noise density in Equation 4.7 can be calculated as $1.16\mu V/\sqrt{Hz}$. We will see in Chapter 5 that the simulated noise levels were very close to the hand calculations.

4.1.2 Gain Stages

The first stage dominates the power consumption because of the noise requirements of the system. Once we extract the signals from the noisy environment, we need to amplify these signals to have enough swing at the output. In order to provide sufficient open-loop gain, it is desired to have enough number of gain stages. Furthermore, it is required to have odd number of stages in the loop gain in order to have negative feedback in closed-loop configuration. The details of the closed-loop system will be explained in Section 4.1.3. Taking into account all these factors, we chose the total number of amplification stages to be three. As an alternative, we could have chosen to have even number of stages at the feed-forward path, and use an additional stage at the feedback loop such as a DC servo loop (DSL) as in [13]. However, since we used very low supply voltage in the design, having two stages would not have provided enough loop gain. On the other hand, having more than 3 stages would result in increased current consumption. Hence, the optimal solution to this was to set the number to three, and have two gain stages after the first stage.

In the design of the gain stages, we followed a similar design methodology with small changes. For instance, we removed the compensation capacitance, C_C, from the second stage due to stability concerns. In addition, we put a Miller capacitor, C_{miller},

between the input and output terminals of the 3^{rd} stage in order to put the dominant pole at the second stage of the amplifier. This was important, since we wanted to isolate the dominant pole. Alternatively, we could have located the dominant pole at the last stage. However, this would not be the best choice, since the load that the amplifier is connected is not a fixed load. Rather, the amplifier is either connected to the ADC or to an output buffer for testing purposes. In order to make sure that the frequency response of the amplifier is not affected by the load that it is connected to, using a Miller capacitor at the 3^{rd} stage, we put the dominant pole to the load of the second stage.

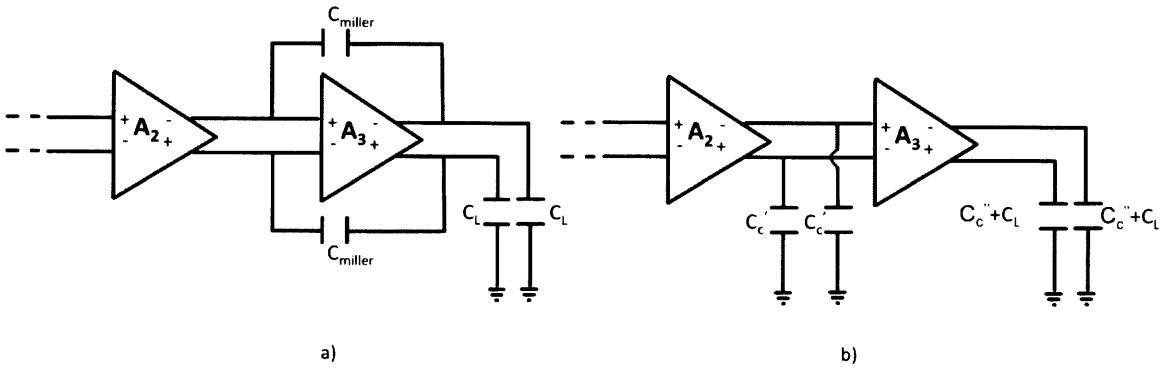

Figure 4-3: a) Location of the Miller capacitor. b)Illustration of the decomposition of the Miller capacitor.

Figure 4-3 shows the location of C_{miller} in the schematics. As shown in Figure 4-3-b, C_{miller} can be decomposed into two capacitors denoted as $C_C{}'$ and $C_C{}''$, where the individual values of these capacitors can be found by using the following equations.

$$C_C{}' = C_{miller}(1 - A_3) \tag{4.8}$$

$$C_C{}'' = C_{miller}(1 - 1/A_3) \tag{4.9}$$

where A_3 represents the mid-band gain of the 3^{rd} stage. As we can see from

Equations 4.30 and 4.9, C_C is multiplied with the gain of the last stage, and becomes a big capacitor C_C' at the load of the second stage. On the other hand $C_C'' \simeq C_C$.

Differential-Mode

Now that we understood the effect of the Miller capacitor, we can write the differential gain expressions for the gain stages by using the similar flow as in the first stage derivations.

$$A_{2,diff} = \frac{A_2}{1 + s/\omega_2} \tag{4.10}$$

$$\omega_2 \simeq \frac{1}{R_{out_2} C_C'} \tag{4.11}$$

At this point, it is important to point out the fact that there is no compensation capacitor at the second stage. This is due to stability concerns at the CMFB loop. Since the second stage output node already presents a low frequency pole due to the Miller capacitor, additional compensation capacitor would create two poles that are close to each other in the common-mode analysis, which could create stability issues.

$$A_{3,diff} = \frac{A_3}{1 + s/\omega_3} \tag{4.12}$$

$$\omega_3 \simeq \frac{1}{R_{out_3}(C_C'' + C_C + C_L)} \tag{4.13}$$

In this derivation, ω_2 appears as a very low frequency pole due to the large value of C_C, and becomes the most dominant pole of our open-loop transfer function. On the other hand, the pole created at the last stage is potentially a low frequency pole due to the low current levels together with the large explicit capacitors in that stage. It is important to set the values of these capacitors, and allocate the current appropriately

in order to separate the poles from each other. We will explain how we set the locations of these poles during the stability and closed-loop analyses.

Common-Mode

The common-mode gain of the gain stages can be found by following a similar procedure as in the first stage analysis. Taking into account the modification in the second stage, where we did not use the compensation capacitor, and using the corresponding small-signal parameters of each stage, the gain values and the dominant zeros at the closed-loop common-mode transfer function for low frequencies can be written by using the following equations.

$$A_{2,com} \simeq \frac{A_2}{1 + g_m R_{out_2} A_A A_B} \tag{4.14}$$

$$\omega_2 \simeq \frac{1}{R_{out_2}(2C_{miller})} \tag{4.15}$$

Similarly for the 3^{rd} stage:

$$A_{3,com} \simeq \frac{A_3}{1 + g_m R_{out_3} A_A A_B} \tag{4.16}$$

$$\omega_3 \simeq \frac{1}{R_9 // R_{10}(2C_{gs_3} + 2C_C)} \tag{4.17}$$

In our design the compensation capacitors at the 1^{st} and the 3^{rd} stages are $50fF$ and $250fF$, respectively, which is set by the constraints coming from the stability as we will explain later. On the other hand, the Miller capacitor has a value of $250fF$ in order to set the bandwidth to the desired value. Using these values and considering the fact that the output resistances at node V_A is chosen to be similar for all the stages, the locations of the closed-loop common-mode zeros turn out to be $12Hz, 62Hz$ and

1 Hz from the calculations. Multiplying the transfer functions of all the stages, we can see that the open-loop gain expression has the most dominant zero around $1Hz$. We will see in the simulation results that the closed-loop transfer function agrees with this result, since the overall feedback in the circuit does not affect the open-loop common-mode transfer function due to the very small forward gain in the open-loop.

4.1.3 Reference Voltage Generation

The reference voltage is used as one of the input voltages of the CMFB block, which is responsible for setting the dc voltage of the output nodes to $V_{DD}/2$. For this purpose, we implemented a switched-capacitor buck converter, which consists of couple of switches and capacitors. Note that, we could also use a simple voltage divider by cascading two pseudo-transistors. However, the output voltage in this case would depend on the matching of the transistors. On the other hand, the switched-capacitor buck converter generates a more reliable reference voltage. The schematics of this block is shown in Figure 4-4.

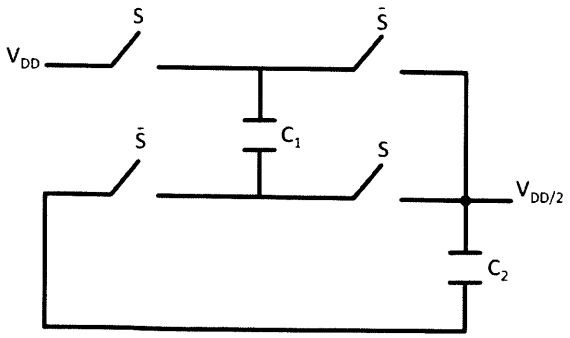

Figure 4-4: Switch capacitor dc-dc converter.

In this figure C_1 represents the flying capacitor, which stores and transfers the energy, where as the capacitance C_2 is the hold capacitor, which holds the output value at the output dc voltage. During the operation, the capacitor array is switched between two phases: the common phase and the gain phase. Figure 4-5 shows the

representation of these two phases. When the charge conversion equations are solved after each cycle, it can be shown that after couple of cycles V_{OUT} converges to $V_{DD}/2$ [36].

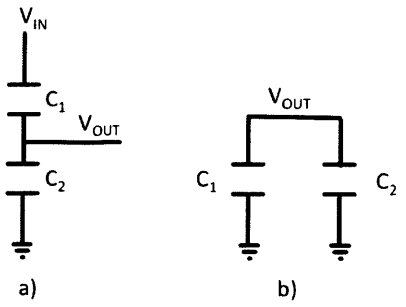

Figure 4-5: Representation of the common and gain phase in the dc-dc converter. a) common phase b) gain phase.

We should note that since the capacitor at the output node is continuously switched between the two states, it is expected to see ripples. The size of these ripples are determined by the time constant at the output, which can be decreased by using a large load capacitance at the output. In our design, we put an extra load capacitance in parallel with C_2 in order to reduce the ripples. In addition to the extra load capacitance, we put an RC-LPF in order to have perfectly smooth reference voltage at the output. The clock of this block was chosen to be the system clock, which was $1kHz$.

4.1.4 Resistor Implementation

The biopotential signal acquisition systems require a high-pass corner ,which is usually set to very low frequencies in order to reject the dc offset and the $1/f$ noise from the system. For EEG and ECG, the cut-off requirements are more strict, since there is significant amount of signal energy between 1-$10Hz$ range. For the sEMG, as we have discussed in Chapter 3, the optimal bandwidth is around 15-$20Hz$, which is higher compared to the other biopotentials. Even though the frequencies of lower cut-off is a

bit higher in EMG, it is still very challenging to create these low frequency poles.

For our amplifier, the high-pass cut-off frequency is created by the feedback capacitor C_2 and the resistor R. The capacitor C_2 cannot be increased too much, since it would decrease the closed-loop gain, or we would have to increase C_1 to even higher values, which would increase the area significantly. Choosing a reasonable value of 200fF for C_2, we can see that the resistor value in order to create a pole around 15Hz is $\sim 50G\Omega$. To implement the feedback resistor that is in the GΩ range, sub-threshold-biased diode-connected transistors, namely pseudo-resistors are utilized instead of bulky passive resistors [5],[37]. Due to its simple architecture, the pseudo-resistor adds small noise and parasitics to the amplifier. In addition, its resistance may change over a large voltage swing. For our system, since we did not have strict high-pass cut-off requirements for our application, the change in the pseudo-resistor over voltage swing was acceptable within certain limits. As we will see from the simulation results, few percent change in the resistance value, which would result in couple of Hz change in the cut-off frequency, was acceptable. The simulated values for the pseudo-resistors will be provided in Chapter 5.

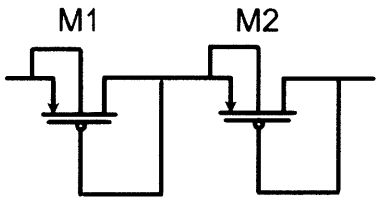

Figure 4-6: Pseudo-resistor implementation [5].

Figure 4-6 shows the pseudo-resistor that we have used in the design of R_P in the common-mode sensing block as well as for the feedback resistor R [5]. We preferred to have two pseudo structures in series in order to double the resistance value. For one of the pseudo-resistors, the approximate resistance value can be derived from the sub-threshold current equation.

$$I_{SD} = \frac{W}{L} I_S e^{\kappa(V_{BG}-V_T)/\phi_t}(e^{-V_{BS}/\phi_t} - e^{-V_{BD}/\phi_t}) \tag{4.18}$$

As shown in Figure 4-6, if the gate is connected to the source, and the bulk is connected to the drain, the equation can be simplified as in Equation 4.19.

$$I_{SD} = \frac{W}{L} I_S e^{\kappa(-V_{SD}-V_T)/\phi_t}(e^{V_{SD}/\phi_t} - 1) \tag{4.19}$$

From this, the resistance can be found by taking the derivative of the V_{SD} w.r.t the current.

$$R = \frac{\Delta V_{SD}}{\Delta I_{SD}} = \frac{L}{W}\frac{\phi_t}{I_{SD}}\frac{1}{[(1-\kappa)e^{(-\kappa V_{SD}+V_{SD}-\kappa V_T)/\phi_t} + \kappa e^{(-\kappa V_{SD}-\kappa V_T)/\phi_t}]} \tag{4.20}$$

If we evaluate this equation by using the approximate values for the parameters, we can see that for small values of V_{SD}, the resistances on the order of $G\Omega$ can be achieved. We verified this model in MATLAB by choosing the values of $\kappa = 0.8$, $V_T = 0.4V$, $I_{SD} = 10^{-18}A$ and $\frac{W}{L} = 4$ to get a resistor value around $30G\Omega$.

We should also note that the matching of the pseudo-resistors, especially for R_P was very important for the CMFB operation. Hence, we used multiple fingers and multiplicities together with common-centroid techniques in the layout of the pseudo-resistors.

4.1.5 Closed-loop Amplifier Schematics

The closed-loop amplifier consists of three stages A_1, A_2, and A_3 as shown in Figure 4-7.

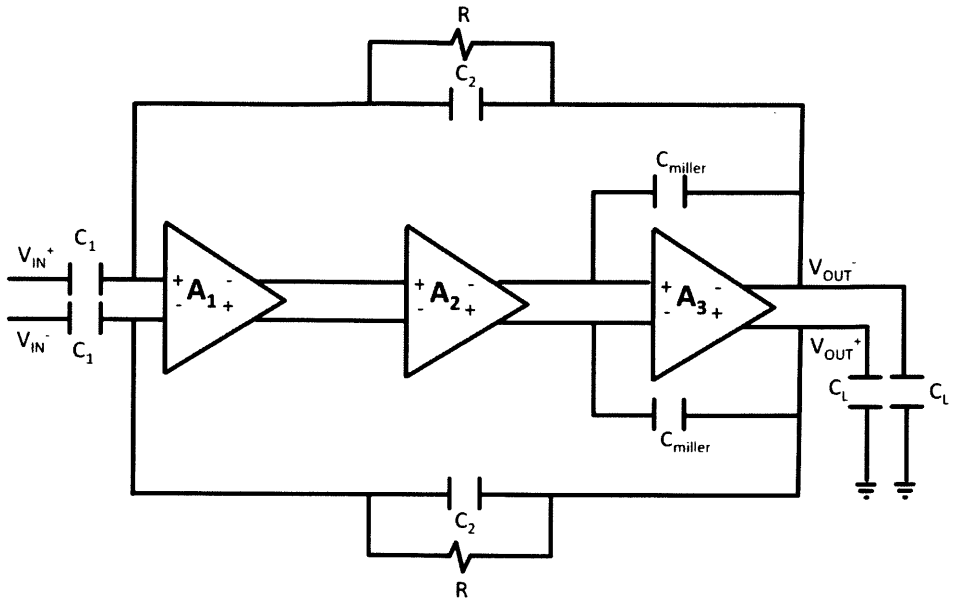

Figure 4-7: Closed-loop amplifier with three stages.

It is an ac-coupled amplifier, where capacitor C_1 provides the ac coupling to the inputs. By this way, any dc offset coming from the electrode interface can be eliminated, and the inputs of the first stage can be independently biased to a desired value. In addition, Figure 4-7 shows the Miller capacitor, C_{miller}, which is used to create the dominant pole of the amplifier as we have discussed before. Furthermore, we see that the feedback path consists of a capacitor C_2 and a resistor R. The capacitor C_2 is responsible for setting the closed-loop gain of the amplifier together with C_1. On the other hand, R_P is a large resistor, setting the bias voltage at the input side to $V_{DD}/2$. We should also note that C_2 and R_P, together, set the high-pass cut-off of the amplifier. We will write the equations in detail once we investigate the block diagram for the overall amplifier.

Figure 4-8 shows the block diagram representation of the closed-loop amplifier. Because of the ac coupling at the input side, there is a transfer function $H_1(s)$ from

the electrode input to the actual amplifier input. $H_1(s)$ has a high-pass characteristics with a very low frequency cut-off, and it approaches to unity gain for higher frequencies. In the forward path, $H_2(s)$ represents the open-loop gain of the amplifier. Finally, the feedback factor β shows the ratio of output signal that is fed back to the input.

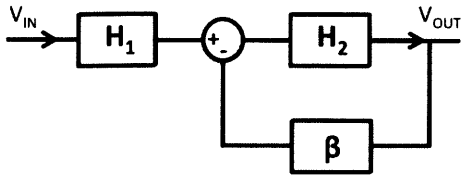

Figure 4-8: The closed-loop block diagram of the amplifier.

Using the notations in Figure 4-7 together with the gain expressions found from Equations 4.2, 4.10 and 4.12, the expressions for $H_1(s)$, $H_2(s)$ and $\beta(s)$ can be written as follows.

$$H_1(s) = \frac{R_p // \frac{1}{sC_2} + \frac{1}{sC_L}}{R_p // \frac{1}{sC_2} + \frac{1}{sC_L} + \frac{1}{sC_1}} \tag{4.21}$$

$$H_2(s) \simeq \frac{A_1 A_2 A_3 (1 + s/\omega_z)}{(1 + s/\omega_1)(1 + s/\omega_2)(1 + s/\omega_3)} \tag{4.22}$$

$$\beta = \frac{\frac{1}{sC_1}}{\frac{1}{sC_1} + R_p // \frac{1}{sC_2}} \tag{4.23}$$

Note that, the zero that is represented by ω_z is created by C_{miller}. It not only puts the dominant pole at the output of the 2^{nd} stage, but also creates a zero at the open-loop transfer function. The value of the zero can be written as in Equation 4.24.

$$\omega_z \simeq \frac{g_m}{C_{miller}} \tag{4.24}$$

We will see that the zero created by this capacitor has been used to improve the phase margin of the amplifier.

Finally, the overall closed-loop system can be modeled by using Equation 4.25.

$$A(s) = H_1(S)\frac{H_2(s)}{1 + H_2(s)\beta(s)} \tag{4.25}$$

From Equation 4.25, we can identify the low-pass corner (f_H), the high-pass corner (f_L) and the mid-band gain (A_{mid}) of the closed-loop system by using the following set of equations.

$$f_H = \frac{1}{2\pi C_2 R_P} \tag{4.26}$$

$$f_L = \frac{\omega_2}{2\pi}(1 + \beta A_1 A_2 A_3) \tag{4.27}$$

$$A_{mid} = \frac{1}{\beta} \tag{4.28}$$

In the design, the feedback capacitors C_1 and C_2 are chosen to be $2pF$ and $200fF$, respectively, which gave us a β factor of $1/100$. Furthermore, the feedback resistor R_P was set to $\sim 50\Omega$ in order to have a f_H around $15Hz$. On the other hand, as we will discuss in more detail when we will do the stability analysis in the following section, the f_L was set to $\sim 450Hz$ by using a ω_2 of $\sim 3Hz$ and using the loop-gain expression that we will derive in the next section.

For the common-mode, we can follow the similar steps in order to find the closed-loop expression. Replacing $H_2(s)$ expression in Equation 4.22 with the common-mode gain values that we have found in Equations 4.5, 4.14 and 4.16, we can find the closed-loop common-mode transfer function. We will provide the simulation results for the common-mode transfer function in comparison with the differential-mode transfer function in Chapter 5, which will give us the information about the CMRR of the amplifier. We will see that the common-mode closed-loop transfer function will agree

with the values that we calculated during the common-mode pole derivations.

Stability

Stability is one of the most important amplifier metrics that needs to be satisfied for proper operation. For multiple-stage amplifiers, it is an issue when the amplifier is used in feedback configuration.

The measure of the stability of the closed-loop amplifier can be seen from the loop-gain characteristics. In our case, the loop-gain, LG, can be extracted from the denominator of $A(s)$ in Equation 4.25.

$$LG = H_2(s)\beta(s) \tag{4.29}$$

As we can see from the Equation 4.29, the LG transfer function is the multiplication of the the open-loop gain $H_2(s)$ and the feedback factor $\beta(s)$. For stability, the phase at which the loop gain is $0dB$ should be greater than $-180°$. Usually, a phase margin of $> 45°$ is desirable for stable operation. In order to better understand our design approach for setting the poles of the system, we can use the diagram in Figure 4-9.

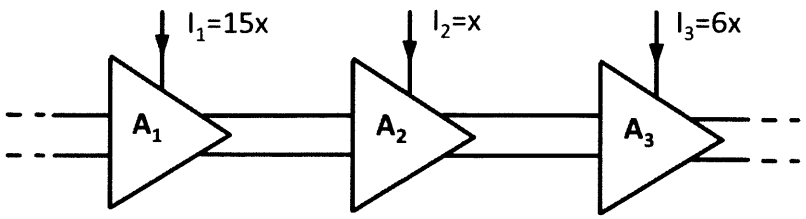

Figure 4-9: The current distribution in the amplifier stages.

The figure shows the relation between the currents at each stage of the amplifier. As a reference, the current at the 1^{st} stage, which is denoted as $15x$, is equal to $1nA$ at each branch of this stage. The approximate current levels in the following stages can be found from the relative ratio of the current levels. It is important to understand the reasoning behind the choice of these current levels.

First of all, as we have discussed in Chapter 3, the 1^{st} stage has to have maximum current in order to stay above a certain noise floor. As a result, the output resistance of this stage is lower than the following stages, which puts the pole created by this stage to high frequencies. In addition, the 2^{nd} stage has the lowest current, since this stage determines the dominant pole of the open-loop transfer function. The reason of using a current level of x is to set the low-pass cut-off frequency to the desired value. As we have seen in the closed-loop amplifier discussion, the desired cut-off for the low-pass corner is $\sim 450Hz$. Since the gain at each stage is around 20, from Equation 4.27, the desired ω_2 can be found as $\sim 34rad/s$. The load capacitor at the end of the 2^{nd} stage can be written from Equation 4.30.

$$C_C{}' = 250fF(1+20) = 5.25pF \tag{4.30}$$

Using Equation 4.11, the output resistance that is required to set the pole location to $\sim 34rad/s$ can be calculated, which requires us to decrease the current level at this stage ~ 15 times compared to the 1^{st} stage.

On the other hand, the 3^{rd} stage should have sufficient current levels in order to have a pole location further from the 2^{nd} stage. From the multiplication of 3 stage gain values, we calculate the approximate dc open loop gain to be $\sim 78dB$. Using the β value of $1/100$, we can see that in order to put the second dominant pole further from the gain cross-over frequency, we need to locate the 3^{rd} stage pole ~ 2 decades after the 2^{nd} stage pole. In order to decide on the current level that we need at the 3^{rd} stage, it is useful to compare the pole expressions in Equations 4.11 and 4.13. Since the total capacitor value at the 3^{rd} stage is ~ 10 times smaller than the capacitor load at the 2^{nd} stage, in order to have the desired pole location, we need to provide ~ 10 times larger current to the last stage. Additionally, if we set ω_z in the open-loop transfer function to a value that is close to the 3^{rd} stage pole location, we can increase the phase around the gain cross-over frequency. In our final design, setting the current

to be 6 times larger than the second stage, we located the zero to be half decade further than the 3^{rd} stage pole. By this way, we guaranteed a phase margin $> 45°$.

The main pole locations that shape the open-loop characteristics in our design are summarized in Table 4.1.

Table 4.1: Approximate pole-zero locations.

$f_2 = \frac{\omega_2}{2\pi}$	$\sim 5.4Hz$
$f_3 = \frac{\omega_3}{2\pi}$	$\sim 320Hz$
$f_1 = \frac{\omega_1}{2\pi}$	$\sim 5000Hz$
$f_z = \frac{\omega_z}{2\pi}$	$\sim 800Hz$

The simulation results for the open-loop and closed-loop transfer functions will be provided in Chapter 5. We will see that the calculated pole/zero locations will be very close to the simulation results. We will observe the slight shift to lower frequencies in the pole/zero locations. This is due to the additional parasitic capacitors that show themselves after the extraction of the amplifier. Furthermore, we will observe the effect of the zero as a bump in the phase response, which will provide sufficient phase margin to the amplifier.

4.2 Motion Artifact Cancellation

In Section 3.1.2, we discussed the conceptual idea behind rejecting the large interference signals. In this section, we will analyze the relevant circuit blocks in detail, and provide the schematics for the logic.

As we have mentioned previously, in order to detect the motion-artifacts, we used a thresholding method, where we got the signal amplitude information from the output bits of the ADC. In order to put the boundaries to the signal amplitudes, we had to decide the maximum EMG signals that we expected to observe. For that purpose, we

used the signal levels that are presented in Figure 1-2 in addition to the measurement results that we collected from our discrete prototype. We saw that the signal levels were mostly between 20μV-2mV for facial sEMG measurements, even though these values were slightly different from person to person. In our future measurements, we are planning to calibrate the system for different people by adjusting the distance between the electrodes. In the calibration process, the maximum signal level will be calibrated to the desired value during maximum-voluntary-contraction [38].

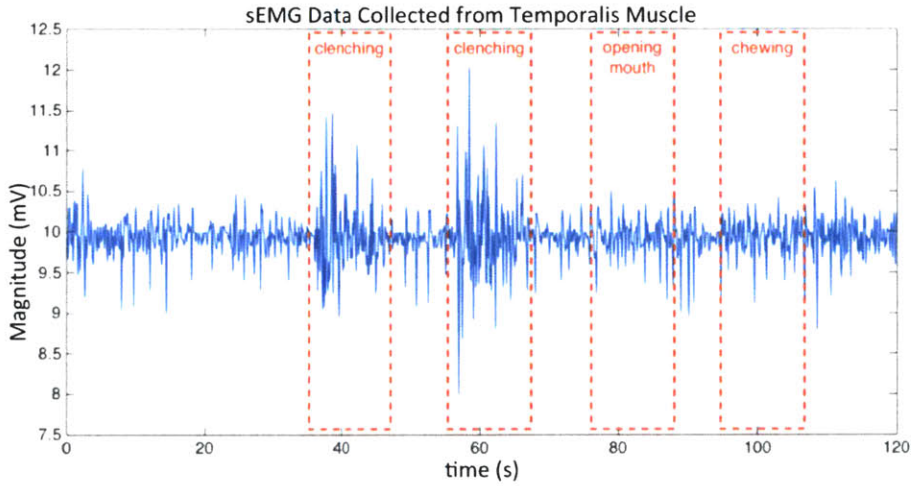

Figure 4-10: Measurement data from the temporalis muscle during activities such as teeth clenching, mouth opening and chewing.

A sample data from the temporalis muscle of a person is shown in Figure 4-10. As shown in that example, the signal levels reach the maximum of $\sim 2mV_{pp}$, when the person is asked to clench her teeth with maximum force. After repeating the measurements for different people, we decided to determine the maximum signal level that we expect to be $3mV_{pp}$.

Since we had a closed-loop gain of $40dB$, the maximum signal level was amplified to $300mV_{pp}$ at the output of the amplifier. The signals above this range were classified as the motion-artifacts. In order to detect this information from the ADC output, we looked at the two most-significant-bits (MSB), namely MSB0 and MSB1. Whenever

both of these bits were either 0 or 1, we made the MAC loop work, and subtract certain amount from the input. This was achieved by a XNOR gate in the logic.

Figure 4-11 shows the details of the MAC topology. The function of the block is to add a fixed step size to the input whenever it falls below the lower threshold, and subtract a fixed step size from the output whenever it exceeds the upper threshold. In the schematic, the NOR gates detect if the signal is out of limits and send the information to the RL bit of the shift register, which decides the direction of shifting. For instance, if the output is above the upper threshold, the NOR gate outputs a 1, which tells the shift register to shift to the right. When it is set to shift to the right, the data-in bit of the shift register becomes DR, which is set to V_{DD}. The V_{DD} at the output of the shift register gets divided by the capacitor divider to set the step size to a desired value, and is sent to the amplifier as an input to be subtracted. The capacitor network consists of an 8 bit DAC. Whenever the output falls down to the limits, the shift register changes its shifting direction to left and the data-in becomes DL, which is a zero. The zero at that clock edge results in a one step decrease at the V_{fb} node. If the signal keeps staying between the thresholds, after 4 clock cycles, the shift register settles, and the MAC loop becomes deactivated. The loop produces the steps in the other direction when the output falls below the thresholds. Furthermore, there are two MAC loops for the two differential inputs. Since the differential signals increase/decrease in the opposite way, the two loops works in the reverse mode.

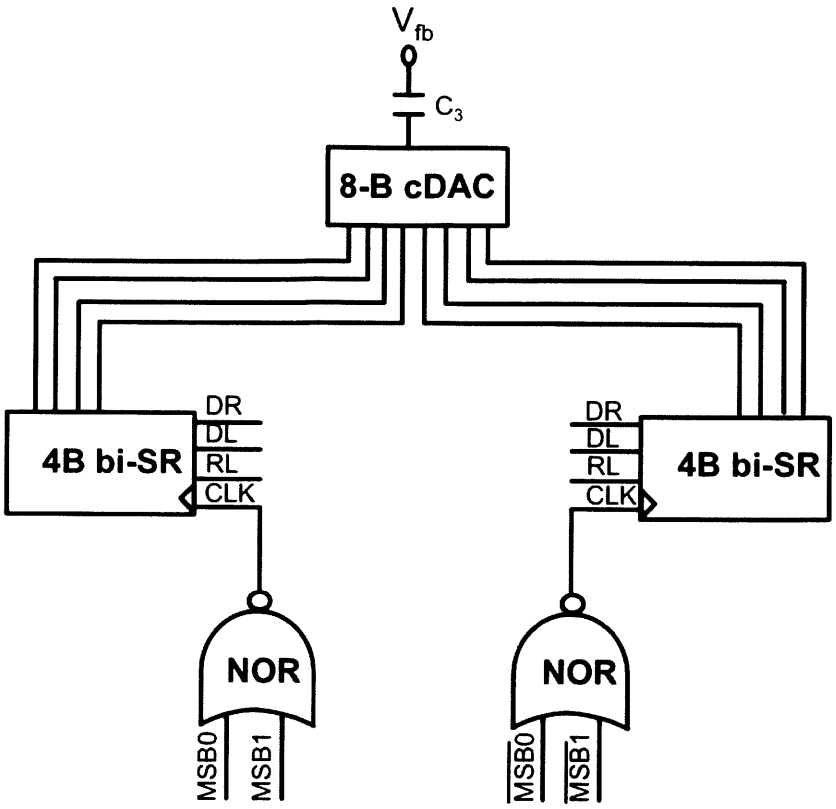

Figure 4-11: Block diagram of the MAC block.

The step size at each clock cycle can be calculated by using Equation 4.31.

$$Step\ size = V_{DD}\frac{C_{DAC}}{8C_{DAC} + C_3} \tag{4.31}$$

where C_{DAC} represents the unit capacitance at the capacitive DAC. There are 8 unit capacitors that are parallel to each other. The step size that is calculated from Equation 4.31 appears as another input to the amplifier. Figure 4-12 shows the visualization of the MAC input together with the amplifier input.

The only difference in the frequency response characteristics of these two inputs is that the mid-band gain for the amplifier is set by the C_1/C_2 ratio, where as for the MAC output, the ratio is C_3/C_2. Other than that, the low frequency and high frequency cut-off frequencies for these two inputs are the same. Choosing the step

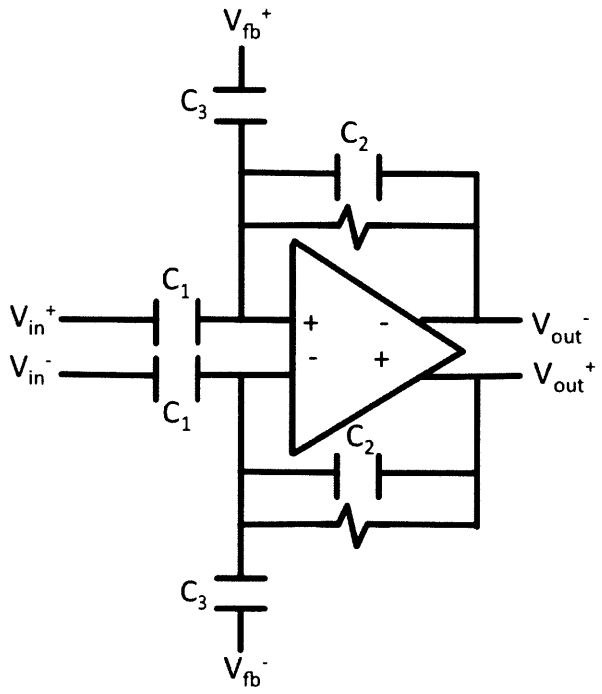

Figure 4-12: The connection of the real signal and the MAC output to the amplifier.

size to be 10mV and setting the C_3/C_2 ratio to 10, we can achieve $\sim 100mV$ step size at the output of the amplifier whenever the MAC loop is active. Considering the fact that the motion-artifact signals are low-frequency signals, this step size would be enough to keep the signal levels between the limits without allowing the signal to rapidly exceed the threshold before the next clock cycle. This could only be achieved, if the clock frequency is set to a high value. However, the upper limit for the clock frequency is set by the bandwidth of the closed-loop amplifier, which is around $500Hz$. Hence, the clock frequency for the MAC loop was set to be $500Hz$. In order to provide this clock, we used a clock divider to generate $500Hz$ from the $1kHz$ system clock.

We should note that the MAC loop was design to reject the motion-artifact signals that are not in common-mode. For moderate common-mode artifact signal levels, the common-mode rejection deals with the suppression of these signals. However, if a very large common-mode signal is present on the electrodes, the MAC loop is not expected to eliminate due to the differential configuration in the implementation. On

the other hand, if the signal levels are within the threshold levels, the MAC loops does not operate or effect the amplification, since the ADC bits disable the block for desired signal levels. Furthermore, the MAC capability can be disconnected from the main amplifier during amplification using the enable pin.

4.3 System Block Diagram

Figure 4-13 shows the system block diagram. As we can see from the figure, the output of the ADC is fed back to the amplifier input by the MAC loops, which are complementary for the differential operation. During the operation, the output of the amplifier is either connected to the ADC or to the output buffer. If the output is connected to the ADC, it needs to go through b_1 buffer in order to be able to drive the ADC properly. On the other hand, if the characteristics of the amplifier is to be tested, then it is connected to the the b_2 buffer, which drives the test load. The details of both of these buffers will be provided in the next following subsection.

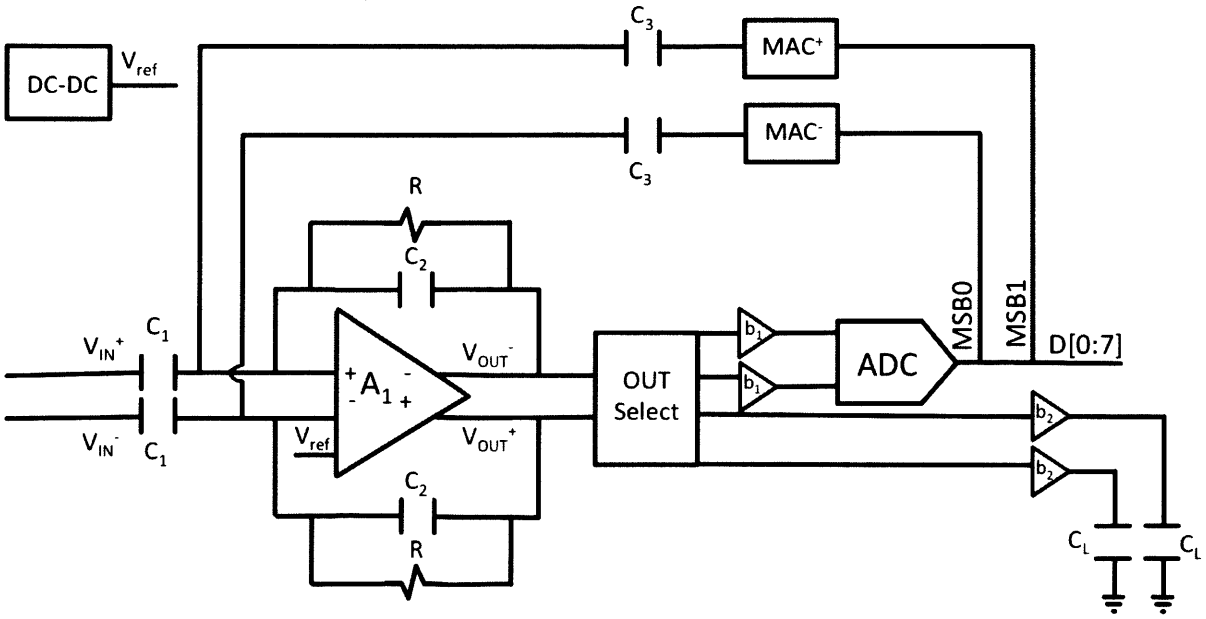

Figure 4-13: System block diagram.

4.3.1 Output Buffer

The output buffer ,b_2, was designed in order to be able to test the amplifier by itself. It was necessary to use this buffer, since the amplifier is not capable of driving large loads. An example load can be the oscilloscope probe, which can be usually modeled as a $10pF$ capacitor in parallel with a $10M\Omega$ resistor. In order to drive such a load, the output stage should provide large current. For instance, for a maximum signal frequency of $500Hz$ and a V_{DD} of $300mV$, the minimum output current can be roughly calculated as follows.

$$I > \frac{300mV \cdot 10pF}{1ms} = 3nA \tag{4.32}$$

Hence, it was necessary to put an additional stage to the output, which provides much higher current to the load. The schematics of b_2 can be seen from Figure 4-14.

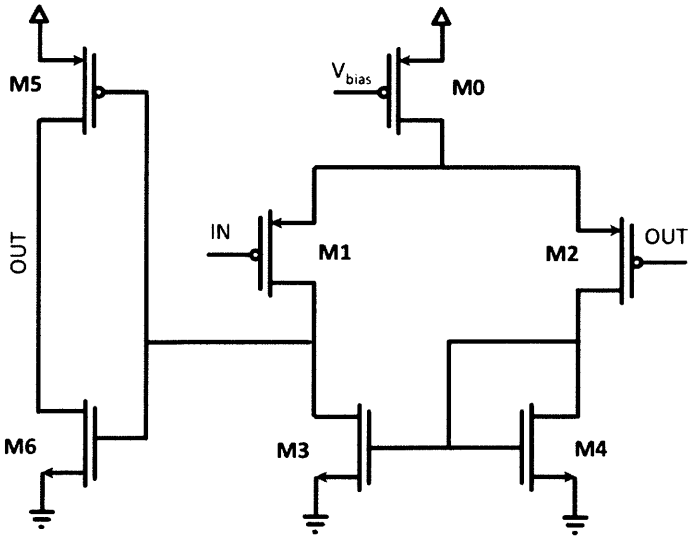

Figure 4-14: Schematics for the output buffer.

It is a two stage OTA, where the output is connected to the negative input in order to operate in the buffer configuration. Different than the whole system, the buffer was driven from $1.2V$ supply in order to provide a current level of around $1\mu A$.

Note that the additional power consumption coming from this block was not added

to the total power consumption of the amplifier, since this block only serves for testing purposes.

4.3.2 ADC Buffer

In order to transfer the output of the amplifier to the ADC input properly, we need to make sure that the amplifier side of the AFE can drive the ADC. At that interface, the amplifier sees the sampling capacitors of the ADC, which in total presents a load of $>700fF$. At each cycle, when the ADC is connected to the amplifier, the amplifier has to charge the sampling capacitors in order to start the signal tracking. However, since the amplifier has few pA at its last stage and has a bandwidth $<500Hz$, it is not able to respond fast enough to the voltage steps at the beginning of each sampling cycle. Hence, we designed an interface for the amplifier-ADC interface. The buffer we put in between the blocks was similar to the output buffer. However, since the ADC buffer was considered to be the part of the system, we were more careful in setting its power consumption. Hence, we used a $0.3V$ supply to reduce the power consumption. This brought us a challenge for the signals close to the rails, since the buffer was not behaving linearly as the output was close to the supply values. In order to solve that problem, we changed the configuration of this buffer to an inverting configuration as shown in Figure 4-15. By this way, even though the signal swing was large, we made the negative input of the amplifier a virtual ground, and managed to work with the buffer for the full range.

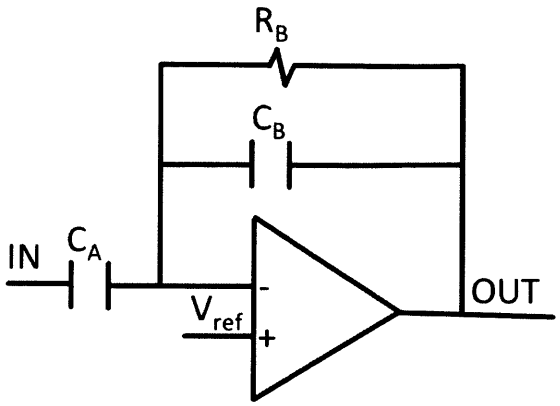

Figure 4-15: Block diagram representation of the ADC buffer.

4.4 Summary

In this chapter, we discussed the details of the circuit design of the AFE. Especially for the amplifier, we provided the small signal analysis, and derived the expressions for the important design parameters. These derivations will be important when we compare the extracted view simulations with the hand calculations in the next chapter. In addition to that, we explained the implementation of the MAC block, and how it was integrated to the system. Finally, we looked into the system block diagram and the buffer designs for different output selections.

Chapter 5

Simulation Results

The AFE was designed in a low power $65nm$ digital CMOS process and has been submitted for fabrication. The chip layout can be seen in Figure 5-1. The total die area including the pads is $2mm$ x $2mm$, while the size of the amplifier is 200μm x 200μm and the size of the ADC is 400μm x 450μm.

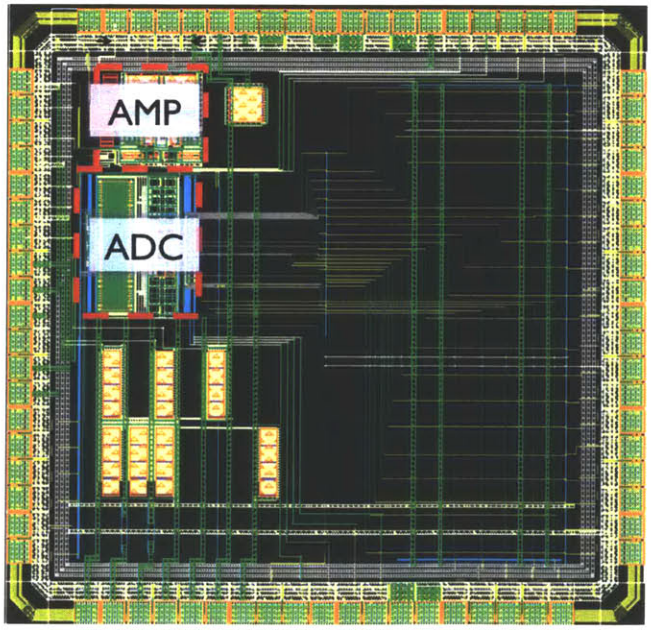

Figure 5-1: The AFE layout in a $2mm$ x $2mm$ die area including the pads.

This chapter will present the simulation results, demonstrating the functionality

and the performance. We will mostly discuss the amplifier performance and provide detailed simulation results for the figure of merit. Furthermore, we will provide system demonstration together with the ADC. We will also investigate the effect of mismatch and process variations on the performance. All presented simulation results will be from post-layout extraction unless otherwise indicated.

5.1 Amplifier

5.1.1 Noise

For the noise simulations, we used the BSIM4 models for SPICE noise analysis. In the model file, there were many options for modeling the thermal noise based on the region of operation. Some models worked best for the above threshold region, where as the other model behaved well for velocity saturation regime or when the short channel effects were dominant. For our simulations, since the transistors were in sub-threshold and the length of the transistors were relatively large, we set the parameters of the noise models that gave us the best approximation to the weak inversion operation. The details of the noise models can be found from the BSIM4 documentation [39].

However, the model that the simulation used for the weak inversion regime was much more complex than the formula that we used in Equation 4.7. In addition to the drain current source that we modeled, the BSIM4 model took into account the gate noise model, which represents the noise current that is flowing from the gate to the source of the transistor [39]. Because of this, the simulated noise was 6% higher than what we have calculated by hand. The simulated input referred noise density can be seen from Figure 5-2.

As we can see from the curve, the input referred noise density at $100Hz$ is around $1.23\mu V/\sqrt{(Hz)}$, where as the hand calculation was found to be $1.16\mu V/\sqrt{(Hz)}$. The flicker noise corner frequency is $\sim 10Hz$, which allows us to make thermal noise limited

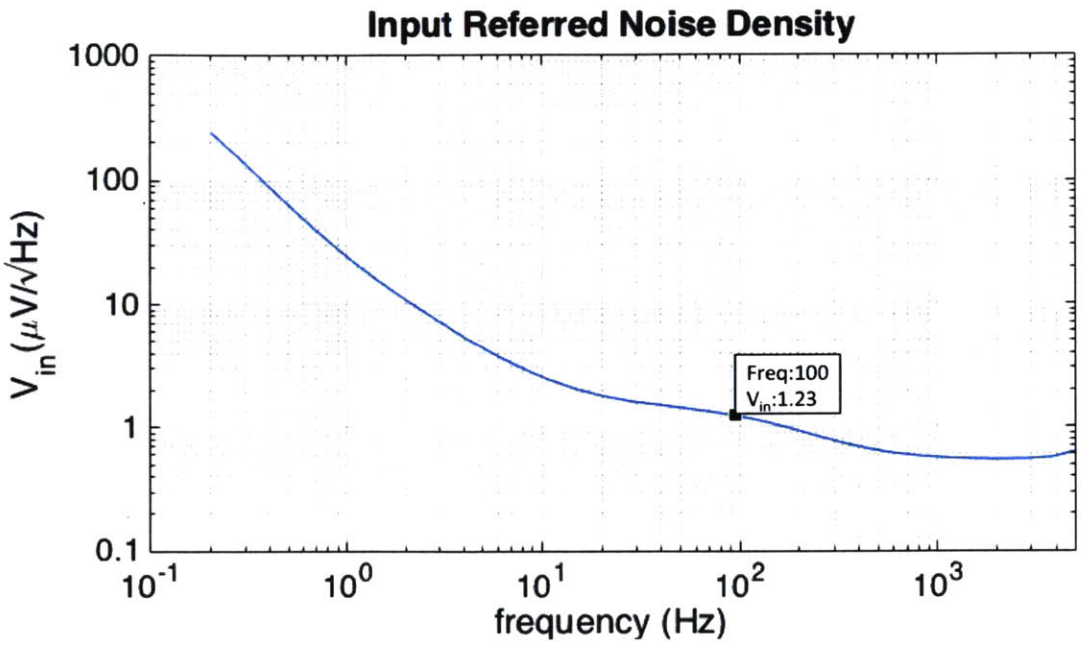

Figure 5-2: Input referred noise density of the amplifier.

behavior assumption for higher frequencies. Also, using the input referred noise density, the equivalent input rms noise can be found as $\sim 25\mu V_{rms}$.

5.1.2 Loop Gain

The loop gain of the amplifier was measured by breaking the feedback loop and finding the transfer function from the input to the point where we opened the loop. As we have discussed in Chapter 4, the phase margin of the amplifier gives the information about the stability of the system, and in general a phase margin of $> 45°$ is desired. From the simulation results, we found the phase margin to be 60° as a result of the bump around the gain cross-over frequency due to the zero in the transfer function. Furthermore, we can see from the figure that compared to the values that we have found in Table 4.1, the pole/zero locations are slightly shifted to lower frequencies as a result of parasitic capacitors coming from the extraction. This will show itself as a lower low-pass cut-off frequency at the closed-loop bandwidth.

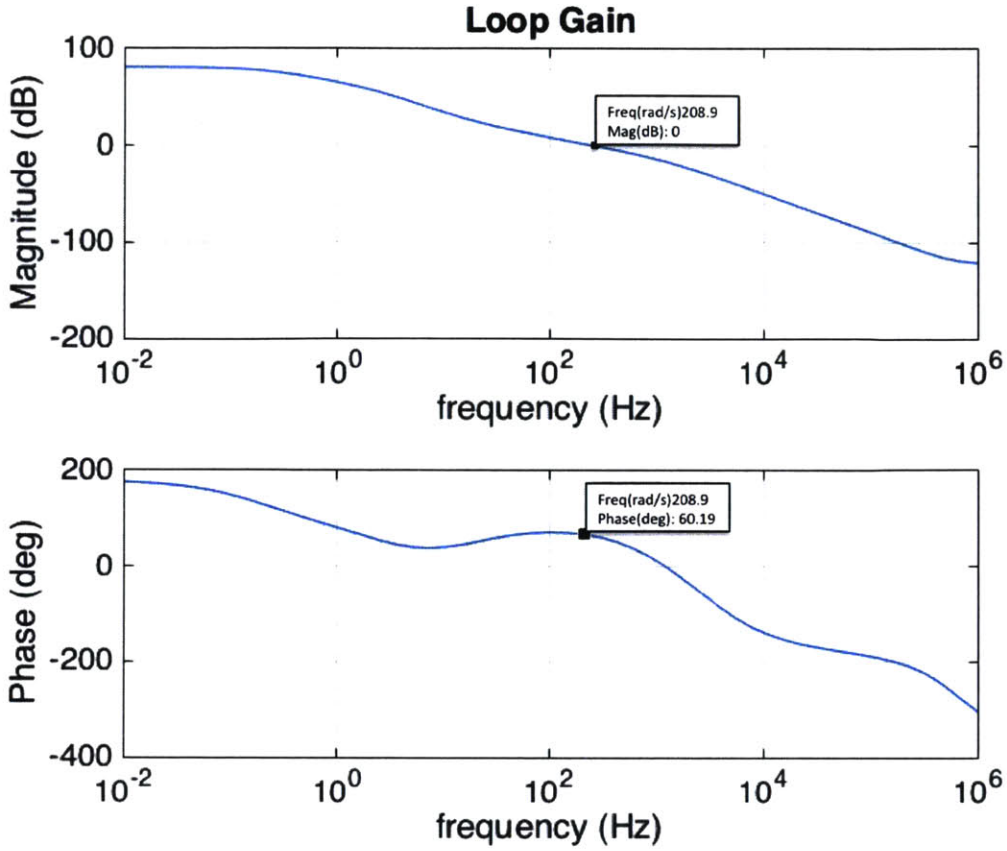

Figure 5-3: Loop gain of the amplifier.

5.1.3 Bandwidth

In Chapter 4, while discussing the closed-loop transfer characteristics, we found the expressions for f_L, f_H, and A_{mid} by using the Equations 4.26 - 4.28. Now, we need to verify and compare the theoretical closed-loop frequency response parameters with the extracted simulation results.

Figure 5-4 shows the closed-loop gain and frequency response of the amplifier for the typical corner. Going back to Chapter 4, from the hand calculations, we found the values of f_L, f_H and A_{mid} to be $15Hz$, $450Hz$ and $40dB$, respectively. We can see from the curve in Figure 5-4 that the extracted view results almost match with our calculations. The location of the f_L is not exact due to the characteristics of the pseudo-resistor R in the closed loop feedback loop. On the other hand, the value of

f_H is slightly lower than the calculated value due to the parasitics added to the output load after the extraction of the amplifier.

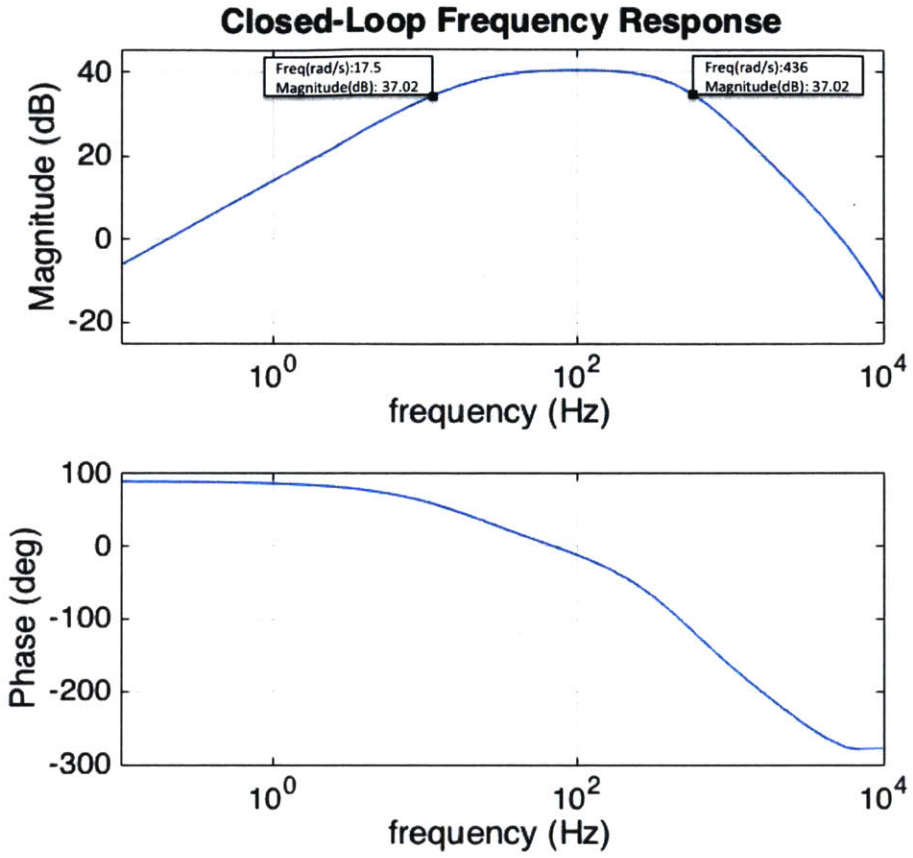

Figure 5-4: Closed-loop frequency response of the amplifier.

5.1.4 CMRR

The CMRR of the amplifier was simulated and compared with the amplifier gain response. The results can be seen from Figure 5-5. As we can see, the CMRR at $60Hz$ was found to be around $85dB$. We should note that after the fabrication, due to the possible mismatches between the transistors, the CMRR value can be degraded from this value.

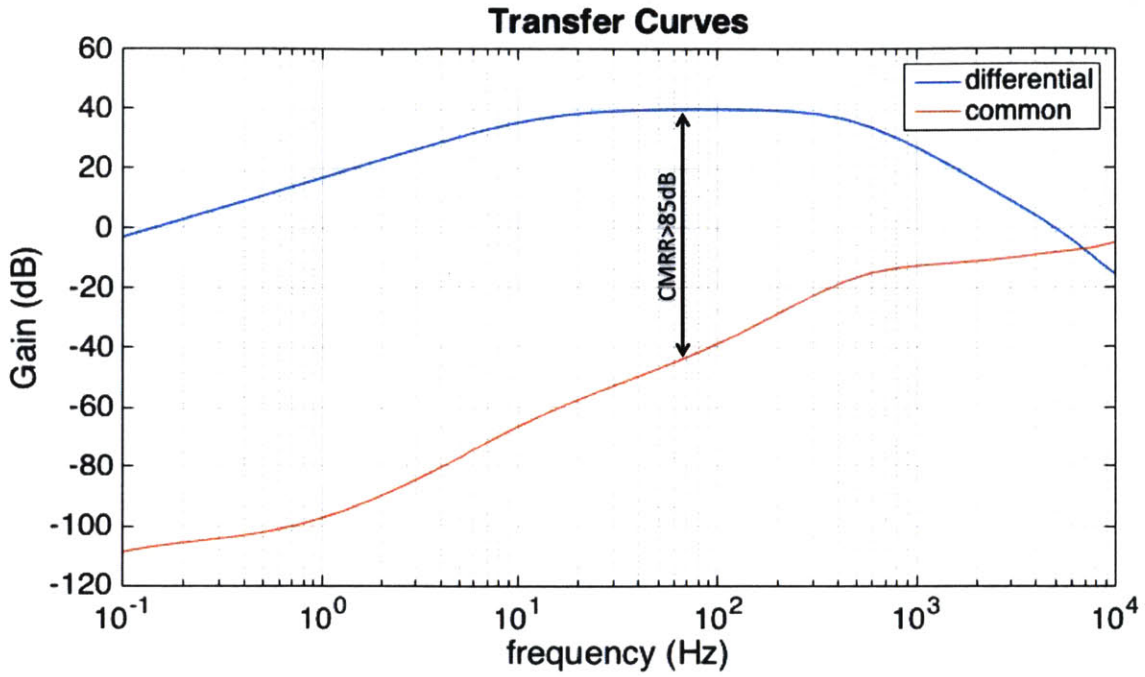

Figure 5-5: CMRR representation of the amplifier.

5.1.5 Step Response

The step response simulation is important in order to test the performance of the amplifier for rejecting the common-mode signals in the presence of both common and differential-mode signals. For that purpose, we gave an input of $60Hz$, $2mV$ common-mode step input together with a differential-mode 40μV sinusoidal signal at 100Hz. The input signals can be seen from the first plot of Figure 5-6.

When we look at the output signal from the second plot in Figure 5-6, we can see that the square wave was attenuated. On the other hand, the differential signal was amplified by the closed-loop gain of the amplifier, and showed itself as a $4mV$ signal at the output. However, even though we do not observe the effect of the square wave common-mode at the output, we see some spikes whenever the step signal toggles. Those spikes are due to the fact that at the instant of switching, the output cannot respond fast enough to reject the common-mode signals, and takes time to settle to the original value, which are expected.

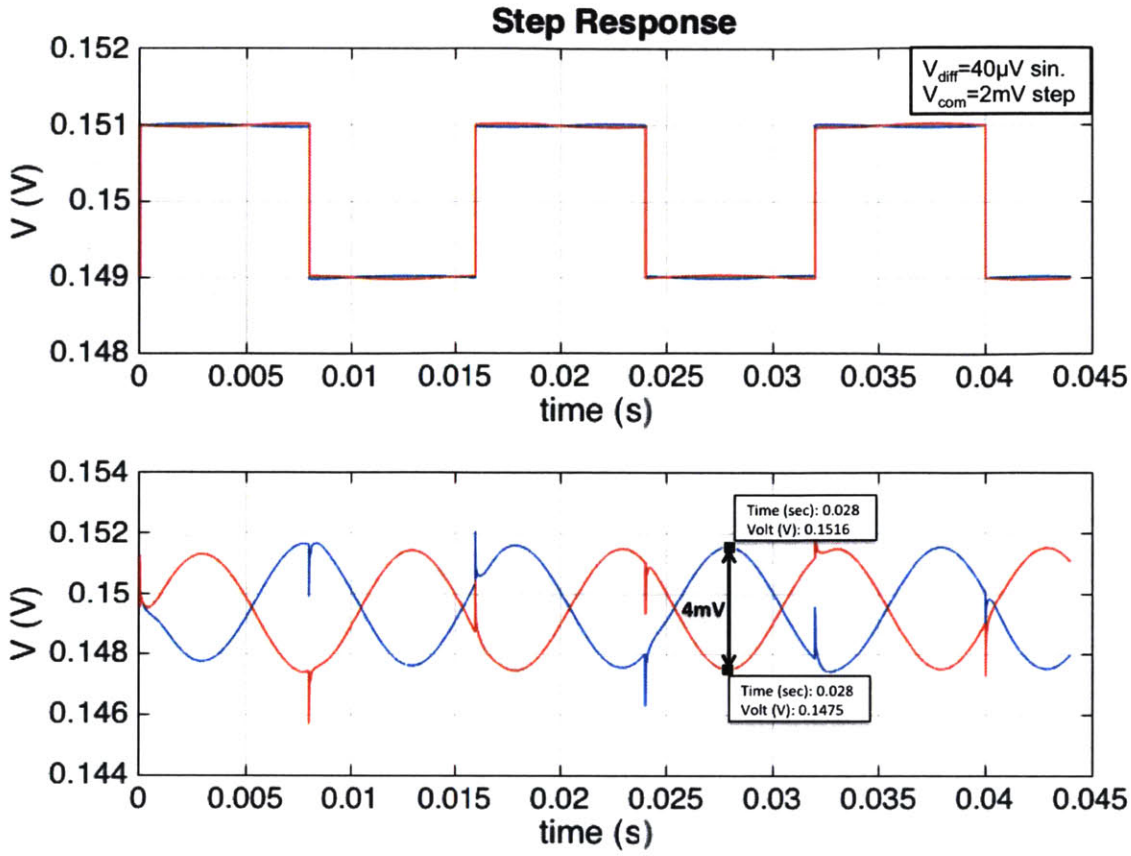

Figure 5-6: Step response.

5.1.6 Power and PEF

For the power consumption simulations, we checked the current flowing through each of the amplifier stages, as well as the additional blocks such as the reference voltage generator and the MAC loop. We verified that the most power hungry block of the system was the first stage of the amplifier, which took $\sim 1nA$ per each branch. On the other hand, the 2^{nd} and the 3^{rd} stage had current levels close to the ones that are represented in Figure 4-9, which in total added up to a total current of $2.8nA$. Taking into account also the current flowing through the DC-DC converter and the MAC loop, the total power consumption of the amplifier was $0.95nW$.

From the current values that we have simulated, we can calculate the NEF and PEF were found to be as follows.

$$NEF = 25\mu V_{rms}\sqrt{\frac{2 \cdot 2.4nA}{\pi \cdot \phi_t \cdot 4kT \cdot 420Hz}} = 2.29 \tag{5.1}$$

$$PEF = 2.29^2 \cdot 0.3 = 1.57 \tag{5.2}$$

5.1.7 Linearity

The testing of the linearity of the amplifier was achieved in two different ways.

First of all, we checked the nonlinearity of the amplifier for the increasing values of the differential signal, when there was no common-mode signal on top of it. This was tested due to the fact that for the large differential input signals, the operating point of the transistors were expected to change with the small signals, especially for the 2^{nd} and the 3^{rd} stage transistors. Furthermore, the large signals might have affected the overall loop gain, and could have caused the loop gain to drop significantly, which would increase the nonlinearity of the closed-loop system. In addition to these sources, the node V_C at the common-mode sensing node is not a perfect virtual ground for the differential-mode signals. Rather, it generates a very small common-mode signal at a frequency of twice of the main frequency of the signal. The generated common-mode signal is not a problem in general for the 1^{st} and the 2^{nd} stage outputs, since the CMFB rejects the generated signals at the following stage. However, for the 3^{rd} stage, since there is no additional stage that would reject the generated common-mode signal at node V_C, we could potentially observe the common-mode signal at the single ended output. However, this is also not a big concern for the nonlinearity, since we measure the outputs differentially. The simulation results for this type of nonlinearity can be seen from Figure 5-7-a. Note that for the testing conditions, we gave no common-mode signal, and we swept the magnitude of the differential-mode signal from $1mV_{pp} - 4.8mV_{pp}$ at $100Hz$. We could have increased the differential input even

more but it would cause clipping at the output.

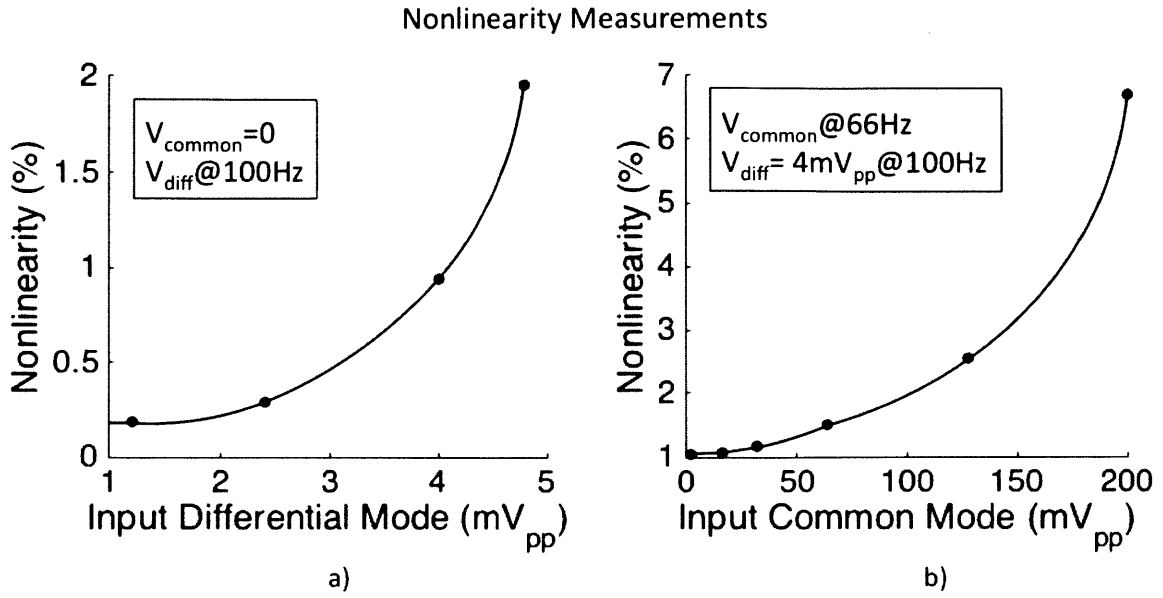

Figure 5-7: Nonlinearity measurements for the amplifier. a) For no common-mode signal. b) With the common-mode signal.

The other simulation for testing the nonlinearity of the amplifier was under the presence of large common-mode signals. The effect here can be explained in a slightly different way than the previous case. For the previous case, the actual input of the first stage was considered as a virtual ground due to the negative feedback configuration of the overall closed-loop. However, for common-mode signals, the input cannot be considered as a virtual ground. Rather, whatever appears at the electrode interface is transferred to the amplifier input. Hence, the nonlinearity of the amplifier starts even at the first stage, and gets amplified by the other stages. As a result, we expected to see more nonlinearity under the presence of large common-mode signals at the input. For the simulation, we gave a fixed input differential signal of $4mV_{pp}$ to the input and increased the magnitude of the common-mode from 0-$200mV$ at $66Hz$. The results can be seen from Figure 5-7-b. When we looked at the output waveform, even for the $100mV$ common-mode interference, the output was still a differential signal and the

CMFB worked fine. Figure 5-8 shows the single-ended output. The numbers in the legend indicate the magnitude of the common-mode signal that was applied on top of the main differential signal. We can observe the distortion at the output for the increasing values of the common-mode.

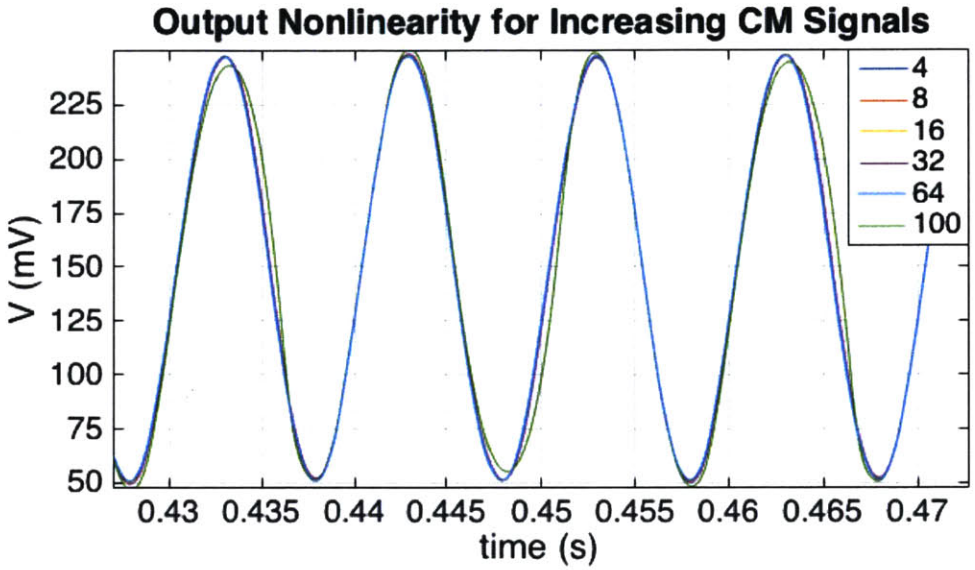

Figure 5-8: The visualization of the distortion for the increasing common-mode voltages.

5.1.8 Corner Simulations

Depending on the process conditions, the fabricated chip can perform better or worse than the typical corner. Hence, we need to verify the functionality of the amplifier for all corners, and if necessary, add some tunability to the critical paths in order to ensure similar performance for all corners. For that purpose, we performed the corner simulations, where the simulator took into account effects such as the threshold change of the transistors for different corners. We observed that for slow corners, the threshold levels were larger, where as for the fast corners the threshold values were smaller than the typical corner. Since we provided the bias voltage of the input PMOS transistor through R in the feedback loop, the current at the stages were set

by the V_{gs} of the transistors, not through a current mirror as in the conventional systems. As a result, when the threshold voltage changed for different corners, the currents deviated exponentially, which was not desired. However, we should note that since all the current levels were set by using the V_{gs} values across the transistors, by scaling the supply voltage for different corners in order to maintain the same over-drive voltage ($V_{gs} - V_T$), we were able to achieve same currents flowing through the stages independent of the process corner. Furthermore, since the CMFB circuits at each stage were also responsible for setting the output DC voltage to $V_{DD}/2$, the feedback mechanism set the output to half supply for any V_{DD} as soon as the correct transistor operation regimes were satisfied. Hence, for the corner simulations, we changed the system V_{DD} from $0.3V$ to specific value depending on the characteristics of the corner. Note that, in addition to threshold tracking, there were circuit-specific conditions that affected the corner simulations. One of the main important factor to keep track was the change in the gain in the CMFB block, which affected the output dc levels, hence the input current. As a result, the voltage scaling is not perfectly correlated with the threshold change. The summary of the values we used can be seen from Table 5.1.

Table 5.1: Corner Simulation Performance Results

	BW(Hz)	Bias current (nA)	Power (nW)	V_{DD} (mV)	HP-select
tt	15-420	1	1	300	1
fs	16-500	1.1	1.1	240	0
sf	6-450	1	0.95	260	0
ff	7-500	0.95	1	360	1
ss	5-450	1	1.2	380	1

In addition to the V_{DD} scaling, we also had to put some tunability to R in the feedback loop, since its resistance directly affected the high-pass cut-off frequency, and this value may change significantly for fast and slow corners. In order to ensure the

same bandwidth across corners, we put a 1 bit high-pass selection bit HP-select.

5.1.9 Monte-Carlo Simulations

The distribution of the input bias current, the power consumption, the DC voltage bias of the input transistors and the output DC voltage was simulated with Monte Carlo analysis. In order to achieve this, the mismatch variation of each transistor in the main amplification path was taken into account during the simulations. A sample graph for the input bias current variation can be seen from Figure 5-9. We can see that for a 1000 point Monte Carlo simulation, the mean value for the input bias current was $1.06nA$, while the standard deviation (STD) was around $70pA$.

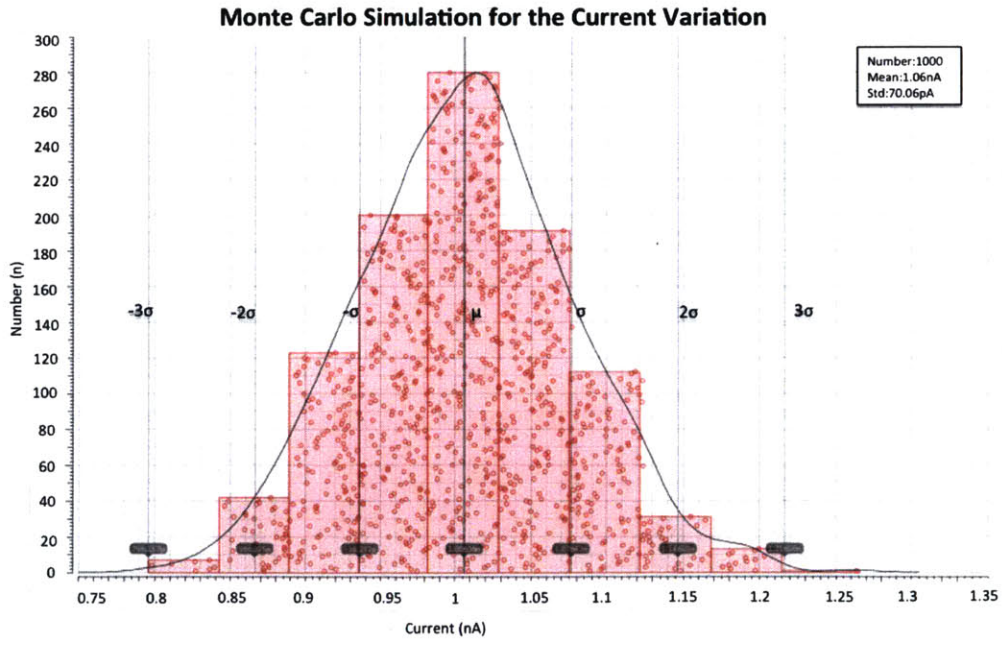

Figure 5-9: Monte Carlo simulation for the input bias current.

Similarly, the mean and the variance for the other parameters are summarized in Table 5.2.

Table 5.2: Monte Carlo Results

Parameter	mean (μ)	std (σ)
Output DC voltage (mV)	149.1	3
Input bias current (nA)	1.06	0.07
Input transistor bias voltage (mV)	152	2.9
Power (nW)	0.96	0.077

5.1.10 Minimum Voltage of Operation

It is important to test the minimum allowable supply voltage for proper operation. In order to achieve that, we decreased the supply voltage from $0.3V$ with $20mV$ steps, and observed the output transient as well as the AC response. The circuit operates properly until $0.1V$ supply voltage. As expected, as we decrease the supply voltage, the current levels drop accordingly, and the noise level increases. However, if the supply voltage is decreased further, the transistors M_7 and M_8 go into cut-off region, and the CMFB block does not work properly. As a result, the DC voltage at the output is no longer $V_{DD}/2$ and the overall open-loop gain drops significantly. This results in a disturbed closed-loop response in the amplifier. Hence, we can say that the minimum voltage of operation is $0.1V$.

5.1.11 Reference Voltage Generation

The switched capacitor DC-DC converter was tested when it was not connected to the amplifier. Note that, since the reference voltage that was created by this block only goes to the gates of the transistors, we do not expect any current flowing through the output of this block. Hence, the results of this simulation would be the same when the reference generator is connected to the amplifier, except for the additional load capacitance that the amplifier introduces.

If we investigate the nominal transfer curve from Figure 5-10, we can see that

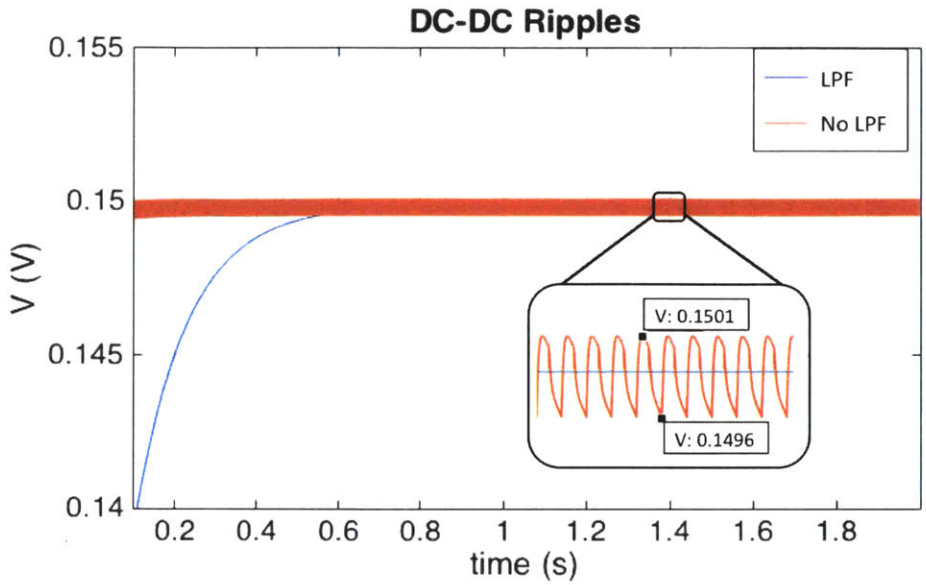

Figure 5-10: DC-DC converter transfer curve with and without the LPF.

the output curve has ripples of around $500\mu V_{pp}$. In order to reduce the ripple size, we could have increased the load capacitance even more. However, we preferred to put a RC-LPF at the output of the DC-DC converter in order to have a smoother transfer characteristics at the output. As we can see from the blue curve in Figure 5-10, the output with the LPF converges to a clean $150mV$ signal with a time constant determined by the RC values used in the LPF.

Figure 5-11 shows the corner simulation for the DC-DC converter. As we can see, the output converges to $V_{DD}/2$ at each corner, even though it converges with different time constants because of the change in the time constant in the LPF for different corners. Note that in the implementation of the resistor in the LPF, we used the pseudo-resistor technique as in the other resistor implementations.

5.1.12 Pseudo-Resistor

The pseudo-resistor simulation was achieved by connecting one side of the pseudo-resistor to a fixed voltage, and by sweeping the voltage at the other end. By measuring the current flowing through the pseudo structure for each ΔV, the resistance value at

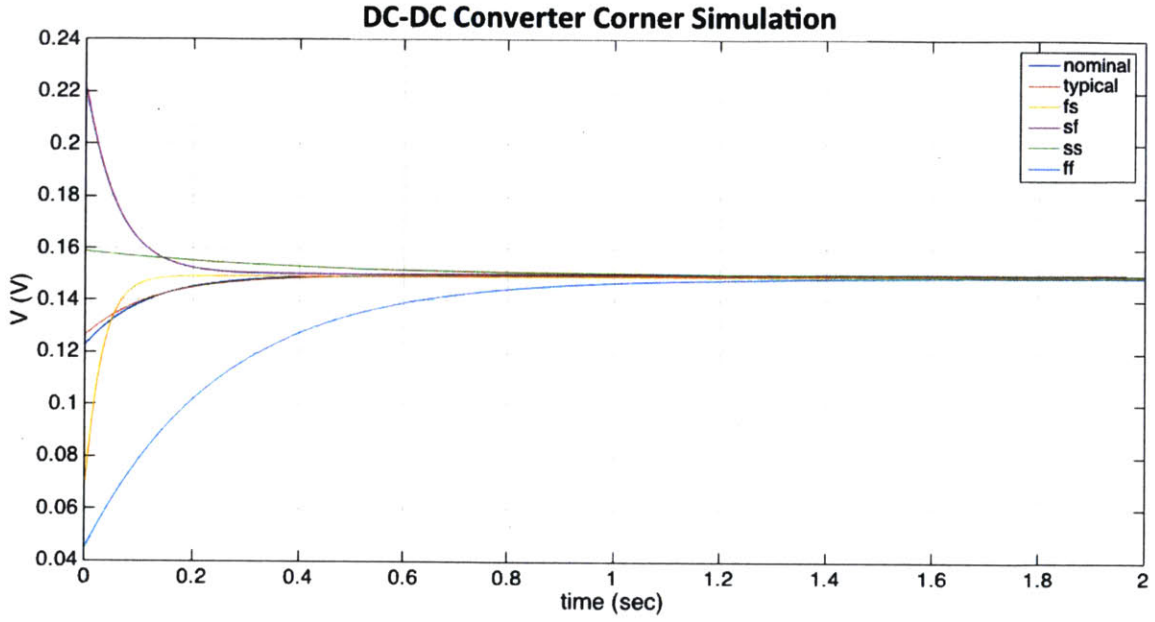

Figure 5-11: Corner simulation for the DC-DC converter.

that condition was found.

For the feedback resistor R in the closed-loop system, the resistance change across voltage was smaller than the change for R_p, which was $\sim 10\%$. This is due to the fact that the $\frac{W}{L}$ ratio of R_p was much larger than R, which caused more current change for a given voltage change across the pseudo-resistor. However, since our only constraint on the value of R_p was it to be very large compared to the output resistors of the individual stages, that much of variation was acceptable. On the other hand, the value of R directly affects the high-pass cut-off of the amplifier, hence its variation should be carefully analyzed. For a ΔV of $+/-0.2V$, the pseudo resistance value changed by $\sim 7\%$, which would cause $\sim 2Hz$ change in the cut-off frequency towards lower frequencies. This is not a significant problem, since the $1/f$ corner frequency is at a much lower value.

5.1.13 Amplifier Performance Summary

Based on the simulation results of the amplifier, we can summarize the figure-of-merit of the amplifier as in Table 5.3.

Table 5.3: Amplifier Performance Summary

V_{DD} (V)	0.3
Power (nW)	0.95
Gain (dB)	40
Bandwidth (dB)	17-435
Input noise (uV_{rms})	25
CMRR (dB)	85
PSRR (dB)	70
NEF	2.29
PEF	1.57

5.2 ADC

The simulation results of the extracted view of the ADC is summarized in Table 5.4.

Table 5.4: ADC Performance Summary

$V_{DD}(V)$	0.3
$Resolution(bit)$	8
$f_{sample}(kS/s)$	1
$FoM(fJ/c.step)$	1.4
$ENOB(bit)$	7.5
$INL(LSB)$	0.1
$DNL(LSB)$	0.1
$Power(nW)$	2.5
$Area(mm^2)$	0.18

5.3 AFE Performance

5.3.1 AFE Transients

In order to test the functionality of the ADC together with the amplifier, we connected the output of the ADC buffer to the ADC inputs, and compared the analog value at the input of the ADC with the digital output value it generated. Figure 5-12 shows an example result from the transient simulations.

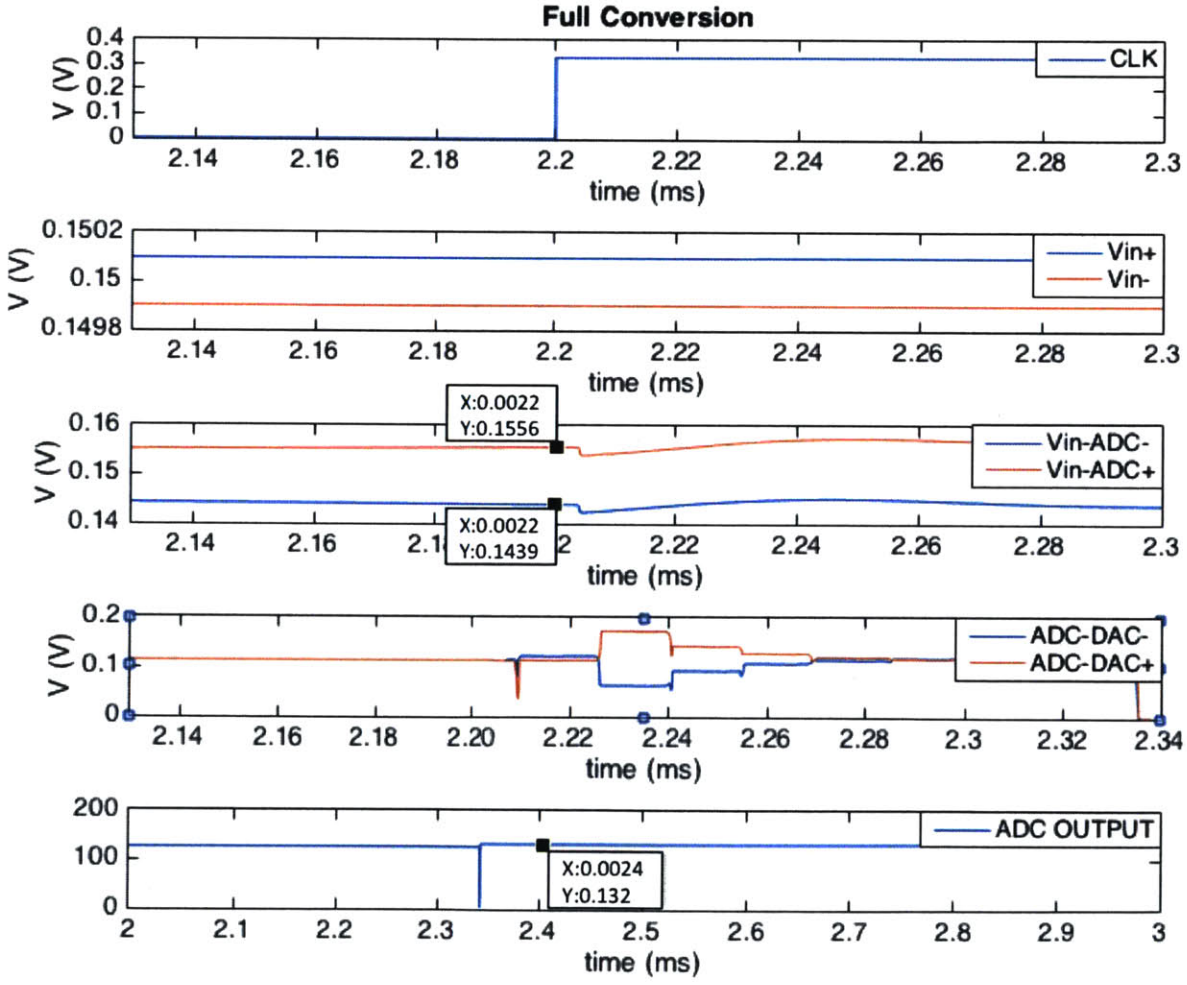

Figure 5-12: Conversion transient.

In the figure, $V_{in}{}^{+}$ and $V_{in}{}^{-}$ represent the amplifier inputs, where as the $Vin_{ADC}{}^{+}$ and $Vin_{ADC}{}^{-}$ represent the output that goes to the ADC input. Right at the positive

clock edge, the ADC samples the values from its inputs and the conversion starts. As the 4^{th} plot shows, the conversion lasts around $800\mu s$, and the ADC outputs the digitized value. From the 8 bit digital value, the ADC output can be found by converting the binary output from the 8 bit DAC to the decimal value. Once we have the digital value, we need to compare it with the expected value, which can be calculated from the analog signal by using the following equations.

$$input = Vin_{ADC}{}^{+} - Vin_{ADC}{}^{-} \tag{5.3}$$

$$attenuated\ input \simeq input \cdot 31/32 \tag{5.4}$$

$$expected\ digital\ output = 128 + \left(128 \cdot \frac{attenuated\ input}{V_{DD}}\right) \tag{5.5}$$

We can see from the Figure 5-12 that the positive clock edge happens at $2.2ms$, where the inputs of the ADC are $155.6mV$ and $143.9mV$, respectively. These are the values that are going to be digitized by the ADC. Hence, we can calculate the expected ADC output by putting the input signal values to the Equations 5.3 - 5.5.

$$input = 155.6 - 143.9 = 11.7mV \tag{5.6}$$

$$attenuated\ input = 11.33mV \tag{5.7}$$

$$expected\ digital\ output = 128 + \left(128 \cdot \frac{11.33}{300}\right) = 132.8 \tag{5.8}$$

Looking at the last waveform in Figure 5-12, we can see that the expected value and the digitized value match.

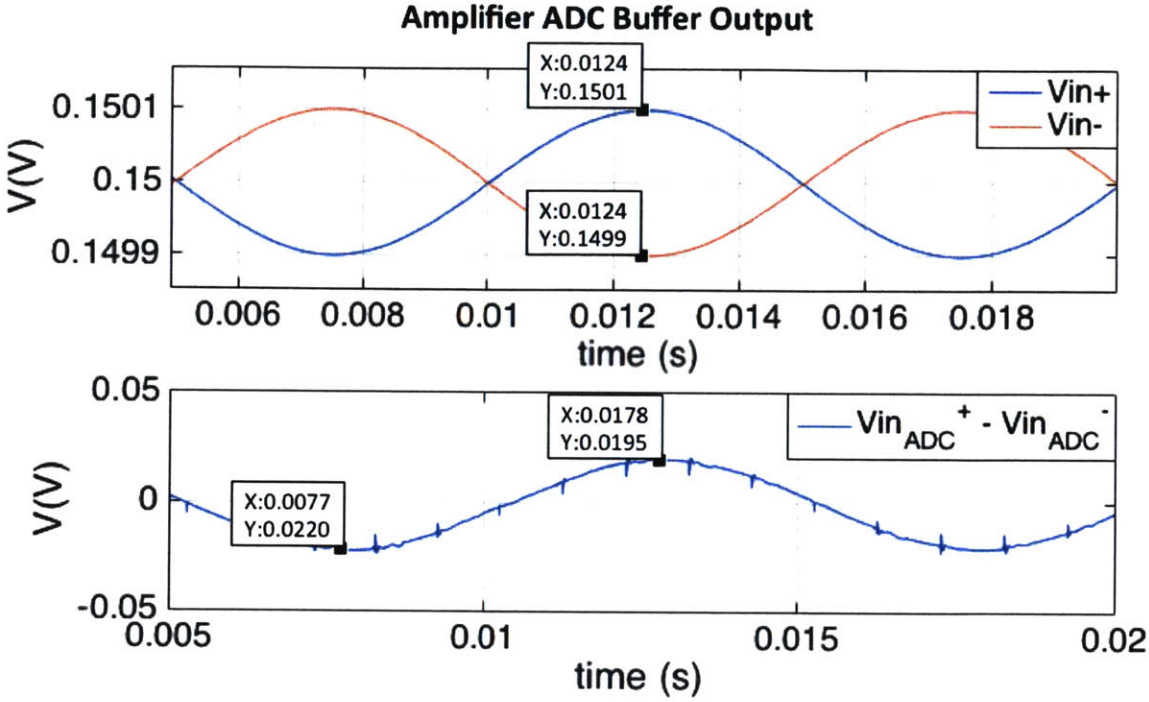

Figure 5-13: Conversion transient showing the ADC buffer output.

In addition to checking the accuracy of the ADC, we should also check the amplification until the ADC input. We can see this from Figure 5-13. The small spikes at the differential output of the ADC buffer is due to the fact that after 200μs from the positive edge of the clock, the sampling capacitors are connected to the ADC buffer output, and at that instant there is no charge on the sampling capacitors. Very quickly, the amplifier responds to that spike and the ADC starts tracking the input. Note that the sampling of the ADC happens much later than the amplifier settling.

5.3.2 MAC

For the functionality of the MAC loop, we will provide the simulation results for the schematics that is shown in Figure 5-14. In this figure, only the half of the MAC circuitry was used in order to show the functionality in a simpler way. The 4 bit bi-directional shift register was connected to the relevant inputs, and the outputs were

connected to the capacitive DAC to create the steps. Finally, a $2pF$ load was used in order to scale the step size similar to the actual system setup.

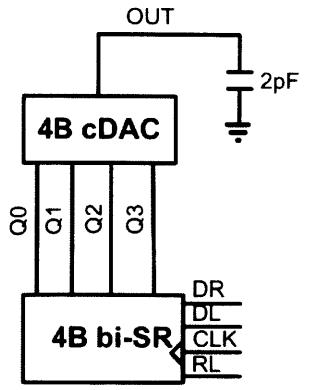

Figure 5-14: MAC test setup.

Figure 5-15 shows the simulation results. The inputs of the shift register were chosen to be a $1kHz$ clock represented by CLK, the RL signal setting the direction of the shift register to right or left, and the input data for the right/left operation denoted as DR and DL. The DAC capacitors were $90fF$ each, and the load capacitor was $2pF$.

As we can see from the figure, when the RL pin is high, the shift register shifts to the right, and uses the DR pin as its input, which is $300mV$ for our case. Hence, after each cycle, one of the shift register outputs toggles to the high output until all the bits are settled. Once the direction bit tells the shift register to shift to left (RL=0), the input data changes to DL=0, and the outputs of the shift register toggle back to ground. Note that during this operation, the shift register has an important role in controlling the direction of the change in the step as well as in providing the gradual change in voltage at each clock cycle. The change in the direction is determined by the comparison of the output of the amplifier with the thresholds.

After each toggle of the shift register, one of the capacitors in the DAC is either connected to V_{DD} or to GND. The step size in this case can be found by using the modified version of the Equation 4.31 for 4 bit operation.

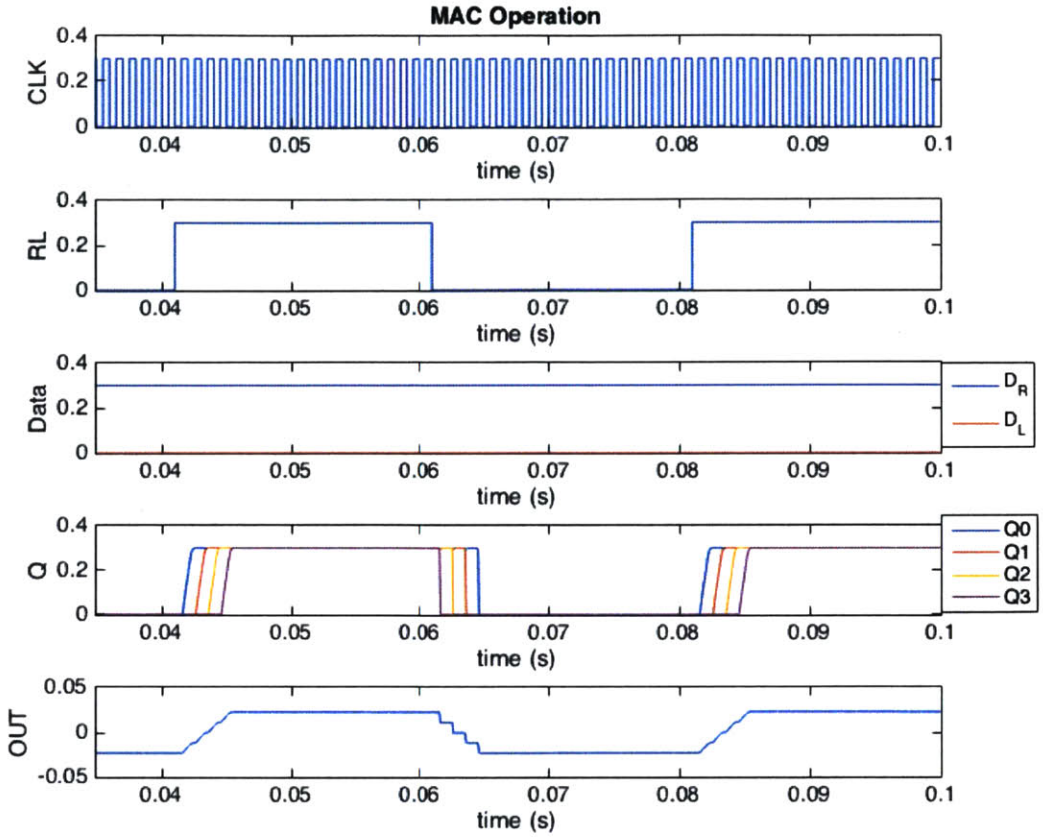

Figure 5-15: Operation of the MAC loop.

$$Step\ size = V_{DD}\frac{90fF}{4 \cdot 90fF + 2pF} \simeq 10mV \tag{5.9}$$

which is exactly the case for the step size at the output signal observed in OUT. This result agrees with the fact that the output of the MAC loop can provide a $10mV$ step at the end of each cycle. That step will get multiplied by the closed-loop gain for the MAC loop, which is set to 10. Hence, at each clock cycle the $10mV$ step that is provided by the MAC loop will be amplified by the gain, and will show itself as a $100mV$ step at the output of the amplifier, if the artifact signal is in the bandwidth of the amplifier. On the other hand, if the motion artifact signal frequency is at a much lower frequency than the high-pass cut-off of the amplifier, that step will also be exposed to the bandwidth characteristics of the amplifier, and be attenuated at

the output.

We can visualize the situation by treating the step as the input signal V_{fb} in Figure 4-12 that is superposed with the actual signal at the input of the amplifier. Different from the main amplifier signal, the step that is fed back to the system will get amplified by the C_3/C_2 ratio, being exposed to the same bandwidth characteristics. On the other hand, if there is no motion-artifact present in the system, no step will be produced, which makes the MAC loop deactivated.

5.4 Summary

In this Chapter, we discussed the simulation results for the extracted view of the AFE. We discussed the performance of the amplifier in detail, and provided the simulated figure-of-merit for the design. We showed that the amplifier achieves ultra-low power consumption of $<1nW$ and still is able to ensure a PEF of 1.57. In addition to that, the amplifier has the ability to reject the large signal artifacts, which can be enabled if desired.

In order to better visualize the novelty in terms of power-efficiency, we can look at the comparison table in Figure 5-16, where we show the PEF versus power consumption of the state-of-the-art biopotential amplifiers together with the simulated amplifier in this work.

As we have mentioned in Chapter 2, for very low power AFEs, it is becoming very challenging to maintain the power-efficiency in the system. We can see this trade-off from the recently published biopotential amplifiers from Figure 5-16. Compared to the state-of-the-art, our simulations have shown that, the estimated AFE performance potentially overcomes the PEF-power trade-off. This was achieved by leveraging low voltage design, and distributing the current to the system in a very efficient way.

Furthermore, we looked at the summary of results for the ADC, and integrated

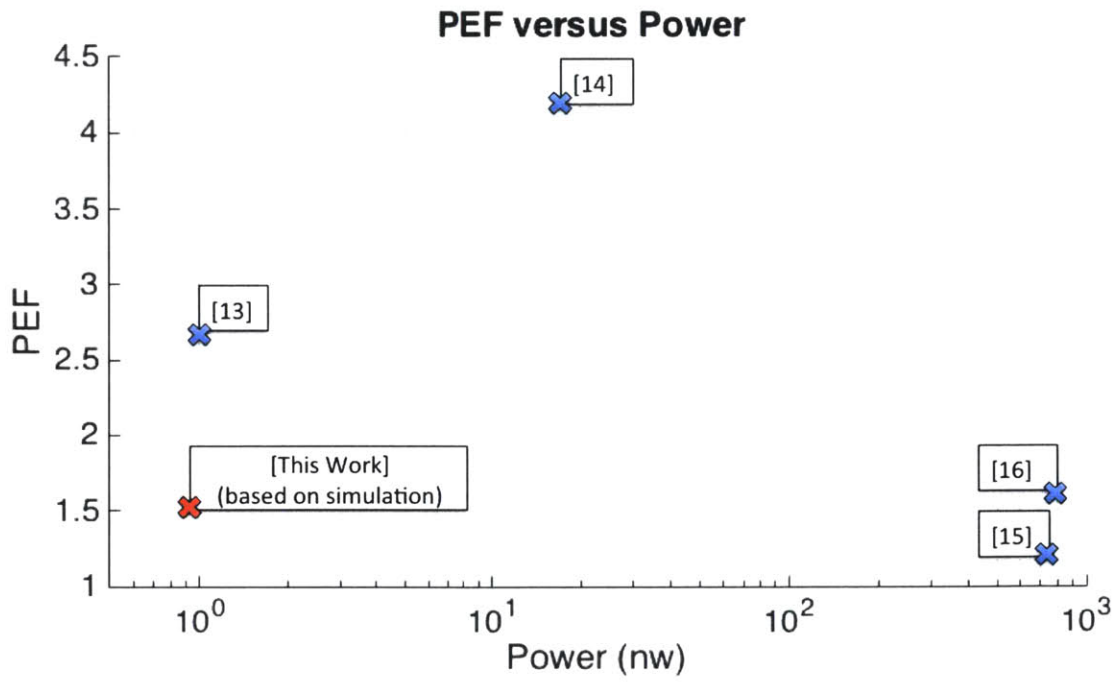

Figure 5-16: PEF versus power comparison of the amplifier with the state-of-the-art.

it to the system simulations. We showed that the ADC is able to provide accurate conversion by consuming $2.5nW$ of power with an ENOB of 7.5 bits. Taking into account the additional $0.6nW$ of power at the amplifier-ADC interface, we can calculate the total power consumption of the AFE to be $4.1nW$. Table 5.5 shows the comparison of the AFE with the state-of-the-art.

Table 5.5: AFE Performances

	[This Work (estimated)]	[13]	[14]	[15]
AFE				
Process (nm)	65	65	65	180
Area (mm^2)	0.22	0.2	0.6	0.25
VDD (V)	0.3	0.6	0.6	0.45
Power (nW)	4.1	3	18.6	940
Amplifier				
Power (nW)	0.95	1	16.8	730
Gain (dB)	40	32	51-96	52
Bandwidth (dB)	17-435	1.5-370	0.5-250	0.25-10000
Input noise (uV_{rms})	25	26	6.52	3.2
CMRR (dB)	85	60	55	73
PSRR (dB)	70	63	67	80
NEF	2.29	2.1	2.64	1.57
PEF	1.57	2.65	4.18	1.2
ADC				
Power (nW)	2.1	1.1/88*	1.8	1350**
Resolution (bit)	8	10	8	9
ENOB (bit)	7.6	9.2	7.14	8.27
INL (LSB)	0.1^+	0.87	1.8	1
DNL (LSB)	0.1^+	0.96	1	0.5
F_{sample} (kS/s)	1	1.1/100*	0.5	200**
FOM (fJ/c.step)	11	1.7/1.5*	25.5	22

$^+$DAC only simulation result. *Performance in integrated system and standalone at max sampling rate respectively [13]. **ADC performance per 10 channels[13].

Chapter 6

Conclusion

A low-voltage, ultra-low power AFE for sEMG signal acquisition has been presented. As a result of exploiting simplistic analog design techniques, the amplifier and the ADC can work from very low supply voltages, yet can achieve state-of-the-art performance. Even though it has a limited power budget, the amplifier is also capable of rejecting the large signal artifacts by using a MAC loop. Together with the ADC, the whole system achieves single-digit nanowatt power consumption. The simulated performance results makes the AFE suitable for applications such as wearable devices and implantable devices, which require long operation lifetime from a small size battery. This chapter summarizes the key results of this research, and suggests opportunities for future work.

6.1 Discussion and Summary of Contributions

The amplifier presented in this thesis has been designed to work with very low supply voltages, which has not been explored much by the analog circuit designers before. As we have mentioned in Chapter 2, low voltage design brought several potential challenges.

One of the main challenges was to ensure proper transistor operation. Since there

is not much voltage headroom for the transistors when the voltage supply is very low, we were motivated to re-design the analog architectures by using as little cascaded transistors as possible. By this way, we relaxed the voltage headroom problem, and managed to keep the transistors in the desired regime during the amplification.

The other problem we dealt with was to be able to keep the NEF and PEF at a low value. This was challenging, since the noise levels increase with the decreasing power consumption in the system. For our case, targeting a nW level power consumption, and keeping the noise floor below $\sim 1.2\mu V/\sqrt{Hz}$ restricted us to allocate most of the current in the system to the first stage, while keeping the current levels at the rest of the system as low as possible. By this way, we managed to present both ultra-low power consumption and state-of-the-art PEF in our system.

Furthermore, the (process-voltage-temperature) PVT variations were a potential problem for our system. We dealt with the effect of the threshold change in the transistors for different corners by scaling the supply voltage accordingly. To reduce the effect of mismatch, we designed the transistors by using large width and length values. In addition, while laying out the transistors, we exploited common centroid techniques and using as many symmetric structures as possible in order to reduce the mismatch in the matched-pairs.

In order to reduce the distortion in the system, we ensured large open-loop gain by using a 3 stage amplifier design, and provided enough headroom for the transistors to keep them in saturation as much as possible during the amplification. The increased number of stages increased the design complexity to satisfy the stability criteria as well as required more current consumption in the amplifier.

In brief, using simple circuit topologies and allocating the current to the system in an efficient way, we managed to scale the power supply without significantly compromising from the performance metrics. The simulated results have shown that the amplifier is able to work with less than $1nW$ power, and still achieves a PEF

of 1.57. As we have seen from the comparison chart in Figure 5-16, our estimated performance overcame the PEF-power trade-off. In doing that, the amplifier provides sufficient gain, which relaxes the number of bits required for the digitization.

Together with the ADC, we present an AFE that is able to work from $0.3V$ supply by consuming only $4.1nW$. The total area of the proposed AFE is $0.2mm^2$. With this power and area levels, the AFE can be integrated to miniaturized signal acquisition systems, and enable long term monitoring for several applications. The chip has been submitted for fabrication and testing is scheduled for Fall 2016.

6.2 Future Work

This section will propose the future work that will be done in order to show system functionality as well to explore the system capabilities for future designs.

6.2.1 User-Study for Data Collection

As we have mentioned before, one of the main goals of this study is to better understand the stress-related health problems by observing the sEMG signals. To achieve this goal, we will use the designed AFE to take measurements from the patients. After getting the Institutional Review Board (IRB) approval, approximately 30 people will be tested during awake and sleeping conditions and the sEMG data will be recorded. In order to improve the conclusions that we will make from the measurements, we will also collect qualitative data from the patients by giving them a survey. The collected data will then be analyzed for feature extraction.

6.2.2 Feature Extraction and Machine Learning Algorithm Development

The observation step will be achieved in the user study, where we collect the related data from the patients. Once we have the data, the understanding part will include the development of machine learning algorithms. First, we will extract the time domain and frequency domain features of the signals that best represent the signal characteristics of the individuals. Then, the machine learning algorithm will be trained by using these feature vectors in order to be able to start making predictions for the next patients. In this process, our aim is to have a system that can estimate the potential problem of a specific patient according to the sEMG signals that are being measured. The representation of the process can be seen from Figure 6-1.

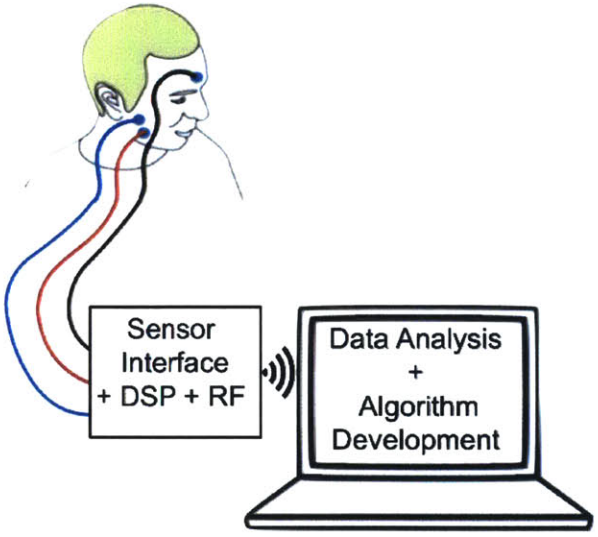

Figure 6-1: Illustration of the data processing.

In the first phase of the algorithm development phase, we will use MATLAB, and do all the classification on the computer. In order to achieve this, we will send the measured data wirelessly by integrating a commercial RF block to the system PCB. We will then analyze the received signals on the computer. Meanwhile, we will explore the alternatives in order to carry the machine learning block to on-chip. This will be

a challenging step since the machine learning algoritms require a lot of computations, which is a concern for the energy efficiency of the overall system. In order to achieve energy-efficient on-chip machine learning, we will explore the ways to simplify the kernels that we can use, which require less computations per task. An example work which focuses on the kernel-energy trade-offs [40] will be a good reference to start with.

6.2.3 Sensor Node Demonstration

Finally, we would like to present a whole system on chip for stress monitoring, that is able to make the real time predictions for the relevant health problems, and be able to have stimulation capability in order to provide relaxation to the patients. The system will be integrated on a sticker type PCB, which will enable the user to easily change the electrodes. Figure 6-2 shows the conceptual representation of the final bio-feedback SoC.

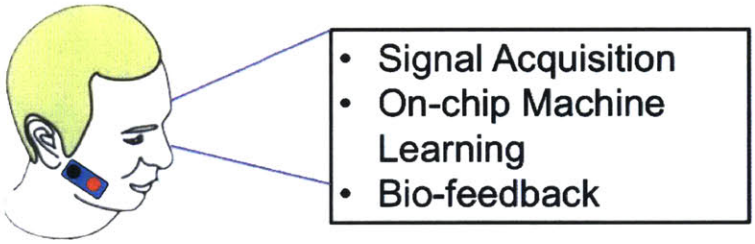

Figure 6-2: The conceptual representation of the finalized system on-chip.

Appendix A

Appendix

ADC: Analog-to-digital-converter

AFE: Analog-front-end

CMFB: Common-mode-feedback

CMOS: Complementary metal-oxide semiconductor

CMRR: Common-mode-rejection-ratio

DAC: Digital-to-analog-converter

DNL: Differential Nonlinearity

DR: Dynamic range

DSL: DC servo loop

DSP: Digital signal processing

ECG: Electrocardiogram

EDA: Electro dermal activity

EEG: Electroencephalogram

EMG: Electromyogram

ENOB: Effective number of bits

EP: Endocohlear potential

FoM: Figure-of-merit

HPF: High-pass-filter

HRV: Heart rate variability

IC: Integrated circuit

ICA: Independent component analysis

INL: Integral Nonlinearity

LSB: Least-significant-bit

LV-LP: Low-voltage low-power

MAC: Motion-artifact-cancellation

MSB: Most-significant-bit

NEF: Noise-efficiency-factor

NMOS: N-channel metal-oxide semiconductor

OTA: Operational transconductance amplifier

PCA: Principal component analysis

PCB: Printed circuit board

PEF: Power-efficiency-factor

PMOS: P-channel metal-oxide semiconductor

PSRR: Power-supply-rejection-ratio

SAR ADC: Successive approximation ADC

sEMG: Surface electromyogram

SNR: Signal-to-noise-ratio

SOI: Silicon-on-insulator

STD: Standard deviation

THD: Total-harmonic-distortion

TMJD: Temporomandibular joint disorder

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