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A. AN ADDITIONAL REALIZATION CYCLE FOR LC IMPEDANCES

Several authors^{1,2} recently have introduced new realization cycles for lossless driving-point impedances. The cycles in question develop the impedance function into unsymmetrical lattices terminated in simpler impedances. In the present report we introduce another realization cycle for lossless impedances, one that develops the impedance into an unsymmetrical bridged tee terminated in a simpler impedance.

The new cycle is shown in Fig. XXI-1. The cycle is appropriate to lossless impedances of the form

$$Z(s) = A \frac{s(s^2 + \alpha_1^2) \dots (s^2 + \alpha_{n-1}^2)}{(s^2 + \beta_n^2) \dots (s^2 + \beta_n^2)} \quad (1)$$

and has associated a remainder function of the form

$$Z_r(s) = H \frac{s(s^2 + \gamma_1^2) \dots (s^2 + \gamma_{n-3}^2)}{(s^2 + \delta_1^2) \dots (s^2 + \delta_{n-2}^2)} \quad (2)$$

The cycle is canonic, since it achieves a four-coefficient simplification of the driving-point function at a cost of four circuit elements.

The procedure for executing the cycle is as follows.

1. Make two total pole removals from $Z(s)$ at infinity, one on the admittance basis, and one on the impedance basis, as shown in Fig. XXI-2.

2. Extract a Brune section from the remainder function $Z_1(s)$ as shown in Fig. XXI-2; select the null frequency ω_o of the Brune section to be any positive real root of the equation

$$0 = 2 \frac{Z_1(j\omega_o)}{j\omega_o} - 2C_o \omega_o^2 \left[\frac{Z_1(j\omega_o)}{j\omega_o} \right]^2 - L_o C_o \omega_o^2 \left[Z_1'(j\omega_o) + \frac{Z_1(j\omega_o)}{j\omega_o} \right] \quad (3)$$

3. Replace the dashed two-port of Fig. XXI-2 by an equivalent two-port of the type shown in Fig. XXI-3. (This can be done conveniently by computing z_{22} for the two-port and then developing $z_{22}(s)$ into a ladder having series capacitors and shunt inductors.)

To establish the validity of the procedure it is only necessary to show that the boxed

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two-port of Fig. XXI-2 is equivalent to a two-port of the type shown in Fig. XXI-3, under the condition (3). This can be done as follows.

Direct analysis of the boxed two-port shows that its impedances take the form

$$z_{22} = \frac{ds^4 + cs^2 + b}{s^3 + as} \quad (4a)$$

$$z_{12} = \frac{es^2 + b}{s^3 + as} \quad (4b)$$

$$z_{11} = \frac{F(a, b, c, d, e)s^2 + b}{s^3 + as}, \quad (4)$$

where the parameters a, b, c, d, e are functions of $C_o, L_o, L, C,$ and $\rho,$ and $F(a, b, c, d, e)$ is a function of a, b, c, d, e which makes the $z_{ij}(s)$ compact at $s = \pm j\sqrt{a}$.

The realizability conditions for the two-port of Fig. XXI-3 are readily found³ to be

- I. The $z_{ij}(s)$ must satisfy the general conditions for lossless realizability.
- II. The $z_{ij}(s)$ must take the form

$$z_{22} = \frac{d's^4 + c's^2 + b'}{s^3 + a's} \quad (5a)$$

$$z_{12} = \frac{c's^2 + b'}{s^3 + a's} \quad (5b)$$

$$z_{11} = \frac{F(a', b', c', d', c')s^2 + b'}{s^3 + a's}. \quad (5c)$$

Clearly, the impedances (4a, b, c) satisfy the foregoing realizability conditions, provided that

$$e = c. \quad (6)$$

Direct calculation shows that (6) amounts to the requirement

$$0 = \frac{L}{C} (\rho-1)^2 + \frac{\rho(\rho-1)L}{C_o} + \frac{L_o}{C}. \quad (7)$$

Substitution of the well-known⁴ values

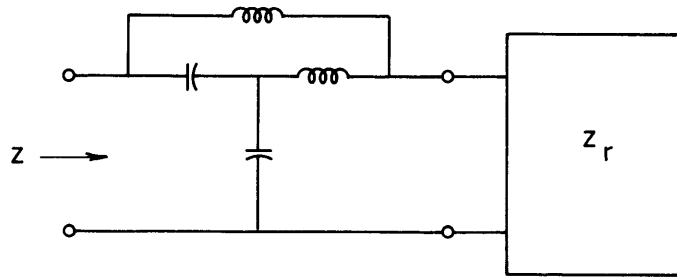


Fig. XXI-1.

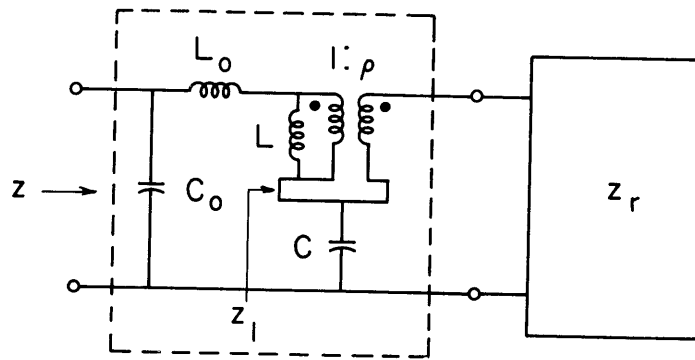


Fig. XXI-2.

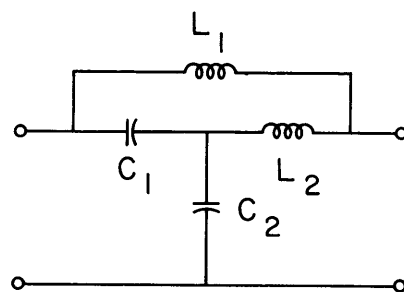


Fig. XXI-3.

$$L = \frac{1}{2} \left[Z_1'(j\omega_0) + \frac{Z_1(j\omega_0)}{j\omega_0} \right]; \quad C = \frac{2}{\omega_0^2 \left[Z_1'(j\omega_0) - \frac{Z_1(j\omega_0)}{j\omega_1} \right]}$$

$$\rho = \frac{Z_1'(j\omega_0) - \frac{Z_1(j\omega_0)}{j\omega_0}}{Z_1'(j\omega_0) + \frac{Z_1(j\omega_0)}{j\omega_0}}$$

and extensive simplification lead to (3). Hence the boxed two-port is equivalent to a two-port of the type shown in Fig. XXI-3, provided that (3) is satisfied.

The following considerations show that (3) admits of at least one positive real solution.

(i) The right-hand member of (3) is a continuous function of ω_0 on the interval $0 < \omega_0 < \omega_1$ (ω_1 denotes the lowest frequency at which $Z_1(j\omega_0)$ has a pole).

(ii) The right-hand member is positive at $\omega_0 = 0 + [\approx 2Z_1'(0)]$, and is negative at $\omega_0 = \omega_1 - \left[\approx -\left(2C_0 k^2 + L_0 C_0 \omega_0^2 k\right) \frac{1}{(\omega_0 - \omega_1)^2}, \text{ where } k = \text{Res} [Z(j\omega_0)]_{\omega_0 = \omega_1} \right]$.

The basic cycle has several variants. These are as follows.

1. The cycle that results when the capacitors and inductors of Fig. XXI-1 are interchanged.
2. The dual of the cycle shown in Fig. XXI-1.
3. The dual of the first variant.

The first variant is appropriate to impedances of form (1), and has associated a remainder impedance of form (2). The second and third variants are appropriate to impedances of the form

$$Z(s) = A \frac{(s^2 + a_1^2) \dots (s^2 + a_n^2)}{s(s^2 + \beta_1^2) \dots (s^2 + \beta_{n-1}^2)}, \quad (8)$$

and have associated remainder impedances of the form

$$Z_r(s) = H \frac{(s^2 + \gamma_1^2) \dots (s^2 + \gamma_{n-2}^2)}{s(s^2 + \delta_1^2) \dots (s^2 + \delta_{n-3}^2)} \quad (9)$$

H. B. Lee

References

1. H. B. Lee, A new canonic realization procedure, IEEE Trans. on Circuit Theory, Vol. CT-10, pp. 81-85, March 1963.
2. R. Yarlagadda and Y. Tokad, On the use of nonsymmetric lattice sections in network synthesis, IEEE Trans. on Circuit Theory, Vol. CT-11, pp. 474-478, December 1964.
3. These conditions can be established by essentially the same line of reasoning as was used by H. B. Lee, loc. cit., to show that (6a,b,c) constitute realizability conditions for the two-port considered there.
4. D. Hazony, Elements of Network Synthesis (Reinhold Publishing Corporation, New York, 1963), Chap. 8, p.140.