1.0 Submicron Structures Technology and Research

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1.1 Submicron Structures Laboratory

The Submicron Structures Laboratory at M.I.T. develops techniques for fabricating surface structures with feature sizes in the range from nanometers to micrometers, and uses these structures in a variety of research projects. The research projects of the Laboratory, which are described briefly below, fall into four major categories: development of submicron and nanometer fabrication technology; deep-submicron electronics and quantum-effect devices; crystalline films on amorphous substrates; and periodic structures for x-ray optics and spectroscopy.

1.2 Microfabrication at Linewidths of 0.1 μm and Below

Joint Services Electronics Program (Contract DAAL03-86-K-0002)
National Science Foundation (Grant ECS 85-06565)
Lawrence Livermore Laboratory (Subcontract 9459005)

Erik H. Anderson, James M. Carter, William Chu, Kazu Komatsu, Hui M. Quek, Anthony Yen, Irving Plotnik, Mark L. Schattenburg, Henry I. Smith

A variety of techniques for fabricating structures with characteristic dimensions of 0.1 μm and below are investigated. These include: x-ray nanolithography, holographic lithography, and reactive-ion etching. Development of such techniques is essential if we are to explore the rich field of research applications in the deep-submicron and nanometer domains. X-ray nanolithography is of special interest because it promises to provide high throughput and broad process latitude at linewidths of 0.1 μm and below, something that cannot be achieved with scanning electron-beam lithography.

[1] M.I.T. Center for Space Research

We are developing a new generation of x-ray masks made from inorganic membranes (Si, Si_3N_4, BN and possibly diamond) and are investigating means for precisely controlling mask-wafer gap, and achieving nanometer alignment. Phase shifting and transform x-ray masks (i.e., in-line x-ray holography) may permit us to achieve sub-50 nm linewidths at finite gaps. A new tri-level technique for making, by electron beam lithography, x-ray masks with linewidths of 50 nm was developed in collaboration with IBM.

Techniques for making x-ray masks from crystallographic templates are being improved. We hope to routinely achieve pattern replication in PMMA with nanometer scale line-edge smoothness.

Achromatic holographic configurations enable us to use deep UV excimer laser sources to produce gratings with finer periods (~100 nm) than are possible with conventional UV laser sources. Although such optical techniques can be used to prepare experimental samples, there are important advantages to using them only for preparing x-ray masks. These masks are then replicated using x-ray nanolithography. With C_k and Cu_L x-ray lithography high-aspect-ratio (almost 8:1) structures with linewidths less than 50 nm have been produced in PMMA.

1.3 Improved Mask Technology for X-Ray Lithography

Semiconductor Research Corporation (Contract 86-05-080)

Salmon Akhtar, Yao C. Ku, Markus Toth, Irving Plotnik, Mark Porter, Henry I. Smith

To utilize x-ray lithography in the fabrication of submicron integrated electronics, distortion in the x-ray mask must be eliminated. Distortion can arise from stress in the absorber, which is usually gold or tungsten. Tungsten is preferred because it is a closer match in thermal expansion to Si, and other materials used as mask membranes. However, W is usually under high stress when deposited by conventional means. We have demonstrated that stress in W can be compensated by ion implantation of Si. Strain-induced deflection of Si_3N_4 membranes was measured in a Linnik interferometer. Stresses of 7×10^9 dynes/cm^2 in W were reduced to zero by implantation of 1×10^{16} Si atoms/cm^2 at 25 keV.

1.4 Theoretical Analysis of the Lithography Process

Semiconductor Research Corporation (Contract 86-05-080)

Henry I. Smith

In an earlier theoretical analysis of lithography we studied the effects of statistical fluctuations on linewidth control, and compared the pixel transfer rates of the various lithographic techniques. This analysis has been expanded to include the effects of nonuniform illumination and other non-ideal factors. We have also derived a method for quantifying process-latitude in lithography, a critically important figure-of-merit in manufacturing. The normalized-process-latitude-parameter was evaluated, as a function of minimum linewidth for several UV and deep UV projection systems, and for an

x-ray system based on a laser-produced plasma source. As expected, the x-ray system showed a significantly larger process latitude in the important linewidth range between 0.1 and 1 μm.

1.5 Studies of Electronic Conduction in One-Dimensional Semiconductor Devices

Joint Services Electronics Program (Contract DAAG-29-83-K-0003)
National Science Foundation (Grant ECS 85-03443)

Dimitri A. Atoniadis, S. Field, Marc A. Kastner, Jerome C. Licini, Udi Meirav, Samuel L. Park, John Scott-Thomas, Henry I. Smith

At low temperatures, Si inversion layers of two-dimensional-electron-gas with widths less than 100 nm in Si, and less than 1 μm in GaAs, become one dimensional. This happens when inelastic scattering is sufficiently reduced that the electronic wave functions have phase coherence over distances larger than the device width.

Three techniques are being employed to fabricate one-dimensional devices. In the first, field-effect transistors are fabricated in Si with widths as narrow as ~50 nm. The narrow gate of these MOSFETs is created by glancing-angle evaporation of tungsten onto a 50-nm high step etched in a 100-nm thick oxide on a Si (100) surface. The tungsten wires are more uniform than those fabricated previously of Al, presumably because of the smaller grain size. In a second technique under development, the inversion layer is created under a narrow slot in a wide metal gate by applying a potential to an upper metal gate separated from the first by a layer of SiO_2. The lower gate with the narrow slot is fabricated using x-ray lithography. To create one-dimensional devices in GaAs we are exploring the possibility of using p-implants to confine the two-dimensional electron gas created by modulation doping or by a gate.

Experiments are underway to characterize these devices at ultralow temperatures using a newly acquired dilution refrigerator.

1.6 Surface Superlattice Formation in Silicon Inversion Layers Using 0.2 μm Period Grating-Gate Field-Effect Transistors

Joint Services Electronics Program (Contract DAAL03-86-K-0002)
U.S. Air Force - Office of Scientific Research (Contract AFOSR-85-0376)

Dimitri A. Antoniadis, Phillip Bagwell, William Chu, Khalid Ismail, Anthony Yen, Marc A. Kastner, Terry P. Orlando, Henry I. Smith

We have been investigating electronic conduction and distinctly quantum-mechanical effects in a surface superlattice (SSL) device. The device is a Si MOSFET with a dual stacked gate configuration. The lower gate is a tungsten grating of 200 nm period (100 nm nominal linewidth), and the upper gate is a uniform metal pad separated from the grating by 200 nm of deposited SiO_2. We call these devices grating-gate-

field-effect transitors (GGFET's). The grating gate is fabricated using x-ray nanolithography and grating contact pads are made with deep-UV lithography. Drain to source current in the SSL device runs perpendicular to the grating wires. A distinguishing feature of our GGFET's is that the strength of the periodic modulation in the channel and the inversion-layer electron density can be independently controlled by external voltage supplies. At low temperatures we observe a modulation of the inversion layer conductance. The conductance variation with gate voltage ($\sim 10^{-5}\Omega^{-1}$) is about one hundred times larger than the universal fluctuations predicted by the theory of Lee and Stone. This is consistent with our suggestion that we are observing diffraction by the imposed periodic potential. We have proposed that the criterion for the observation of lateral surface superlattice effects is that the electronic wave functions be phase coherent over distances longer that the period of the grating. That is, that the inelastic diffusion length be larger than the period.

The first generation of devices had low fabrication yields due to poor gate contacts, adhesion problems, metallization problems and shorts to the substrate. Devices also had low mobility due to radiation damage. These problems have been resolved and a new processing sequence for the second generation devices has been developed.

1.7 Study of Surface Superlattice Formation in III-V Field-Effect Transistors

U.S. Air Force - Office of Scientific Research (Grant AFOSR-85-0376)

William Chu, Khalid Ismail, Dimitri A. Antoniadis, Marc A. Kastner, Terry P. Orlando, Henry I. Smith

In this project we are developing a surface superlattice (SSL) FET device based on the AlGaAs/GaAs heterostructure. This device will allow us to subject a high mobility two-dimensional-electron gas to a field-controlled SSL, similar to that in the silicon grating-gate MOSFET discussed in Section 1.6 of this report. The silicon GGFET device has exhibited reproducible "structure" in the drain current (and transconductance) vs. gate voltage curves at liquid helium temperatures. This structure was attributed to "quasi-mini-gaps" in the energy band diagram caused by the periodic potential of the grating gate. Since their mobility in silicon is low, electrons do not travel much more than about 0.2 μm (which is comparable to the grating period) at a few degrees Kelvin before suffering an inelastic collision and thereby losing phase coherence. If an electron could travel several grating periods between inelastic scattering events, the surface superlattice effects should be much stronger. Such long inelastic lengths can be achieved in high electron mobility (HEMT) devices even at liquid nitrogen temperature. If the expected quantum effects are inherent to surface superlattice devices, then the effect observed in a Si GGFET at 1.2K should appear in the characteristics of a HEM-GGFET at 77 K and perhaps above, due to the substantially higher mobility of the latter device.

To get a better understanding of the HEMT, which is the basic block in building surface superlattices on III-V compound materials, our device structure has been simulated in the semiclassical limit. Many of the effects we anticipate from our HEM-GGFETs (e.g., Block oscillations, quantum tunneling, etc.) will need to be simulated in the quantum regime, which we are not yet able to do. Nevertheless, a semi-

classical simulation of the HEMT based on the solution of Boltzmann's transport equation is very helpful to get the required thickness of layers and doping levels. At this time, devices are in fabrication using processes similar to those for the Si GGFET, appropriately modified for GaAs/GaAlAs heterostructures.

1.8 Investigation of One-Dimensional Conductivity in Multiple, Parallel Inversion Lines

Joint Services Electronics Program (Contract DAAL03-86-K-0002)

Phillip Bagwell, Anthony Yen, Dimitri A. Antoniadis, Marc A. Kastner, Terry P. Orlando, Henry I. Smith

To study one-dimensional conductivity without the statistical fluctuations normally associated with small systems, field-effect devices have been fabricated that use a submicron-period grating-gate structure to produce 250 narrow inversion lines in parallel. The device is fabricated on the same substrate and by the same procedures as the Si GGFET's discussed elsewhere in this report. In fact, the major difference is that the grating lines are now parallel to the electron flow. Others have reported a variety of devices which produce a single narrow "micro-channel," but the expected quasi-one-dimensional density of states has been obscured by large random fluctuations inherent in small systems. Here, the parallel measurement of many such one-dimensional conductors results in an improved signal-to-noise ratio in the density-of-states sampling. This is due to the incoherence of random fluctutations in different micro-channels in the same device. Proper independent biasing of the two gate electrodes results in the formation of a parallel array of 50 to 100-nm-wide lines of inversion charge connecting the source and drain. Transconductance measurements demonstrate a weak, regular modulation that is consistent with the expected quasi-one-dimensional density-of-states.

1.9 Study of Electron Transport in MOSFETs in Si with Deep-Submicron Channel Lengths

Joint Services Electronics Program (Contract DAAL03-86-K-0002)

Ghavam Shahidi, Dimitri A. Antoniadis, Henry I. Smith

Electron conduction in sub-100-nm channel length, Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) in Si is being studied. The devices were fabricated with a combination of x-ray and optical lithographies. The x-ray mask, which defined the minimum lithographic features, was fabricated with conventional photolithography, anisotropic etching, and oblique shadowing. The gate oxide thickness for these devices was 7.5 nm. Electron velocity overshoot, to values exceeding 10^7 cm sec^{-1} at room temperature and 1.5×10^7 cm sec^{-1} at liquid nitrogen temperature, was observed for the first time. Last year we reported electron velocity overshoot in MOSFETs with 95 nm channel length at liquid helium temperature. No evidence of overshoot at 77 K was found in those devices. Our present devices are similar to those in the earlier report, with the exception that the doping in the inversion layer is now about 10^{16} cm^{-3} instead

of $5x10^{17}$ cm^{-3}. Control of punchthrough is achieved by a boron implant in the channel of $4x10^{12}$ cm^{-2} at 50 keV. After oxidation at 900° C for 10 min in O_2, to grow the gate oxide, the boron profile remains abrupt with a peak concentration of about $2.2x10^{17}$ cm^{-2} at 0.19 μm depth. The low-field mobility was estimated from long channel MOSFETs on the same substrate to be about 450 cm^2/Vsec.

From our experiments we conclude that electron velocity overshoot must be taken into account when modeling electron transport at high electric fields in devices with relatively low doping concentration.

1.10 Application of the Shubnikov-de Haas Oscillations in Characterization of Si MOSFETs and GaAs MODFETs

Joint Services Electronics Program (Contract DAAL03-86-K-0002)

Stephen Y. Chou, Dimitri A. Antoniadis, and Henry I. Smith

The Shubnikov-de Haas magnetoconductance oscillations were used to measure directly the gate-to-channel capacitance of Si MOSFETs and GaAs MODFETs, detect the onset of parallel conduction in GaAs MODFETs and to provide an approximate measure of channel length in the sub-100-nm channel of Si MOSFETs. The measurements do not require knowledge of any device parameters, are immune to any gate parasitic capacitance, and are independent of source and drain series resistance. One needs to know only the magnetic field, the oscillation period (for gate-to-channel capacitance measurement), the gate voltage (for detection of the onset of parallel conduction), and the number of oscillation peaks (for the channel length charcterization). Experimental results have shown that the characterization methods are accurate, and can be applied to FETs with sub-100-nm channel length.

1.11 Crystalline Films on Amorphous Substrates

National Science Foundation (Grant ECS 85-06565)

Sergio Ajuria, Harry A. Atwater, Jerrold A. Floro, Stephen M. Garrison, Joyce E. Palmer, Hui M. Quek, Henry I. Smith, Carl V. Thompson

The development of methods for producing crystalline films on amorphous substrates is an important aspect of our program. This is motivated by the belief that the integration of future electronic and electrooptical systems will be facilitated by an ability to combine, on the same substrate, a broad range of materials (Si, III-V's, piezoelectrics, light guides, etc.). Zone melting recrystallization (ZMR) has been highly successful, but device-quality films are obtained only at the expense of high processing temperatures since the material of interest must be melted. ZMR has been an important testing ground for materials combination, and for a number of novel concepts based on the use of lithography to control in-plane orientation and the location of defects. In this year, an improved ZMR apparatus was built which permits the solidification front to be monitored with a video camera. Several distinct interface morphologies were observed

and a theory developed which explained the morphologies on the basis of dynamic balance between absorption of light by solid Si and reflection by molten Si.

The most promising approach in the long-term to crystalline films on amorphous substrates is, in our view, based on surface-energy-driven secondary grain growth (SEDSGG). In this approach, no melting or phase change occurs. Instead, we take advantage of the very large surface energies inherent in ultrathin (~20 nm) films to drive the growth of large secondary grains having specific crystallographic planes parallel to the surface. This phenomenon has been demonstrated, as has the use of very fine gratings (~100 nm linewidths) to control the in-plane orientation (i.e., graphoepitaxy in combination with SEDSGG). Currently, research is focused on basic studies of grain growth phenomena in ultra-thin films and means for promoting grain growth at temperatures many hundreds of degrees below the melting point. Theoretical models for surface-energy-driven secondary grain growth were developed and have, for the most part, been confirmed by experiments on Si, Ge and Au films. Both ion bombardment and intense optical irradiation enhance grain boundary mobility. In the case of Ge thin films, self implantation at 500°C with 30keV Ge ions achieves a grain growth that by thermal annealing would require 775°C. In thin films of gold, secondary grain growth occurs at room temperature as soon as the film becomes continuous (at ~18 nm). Low energy Ar ion bombardment enhances grain-boundary mobility in Au. In films of Ge 30 nm thick we achieved graphoepitaxial orientation by the purely solid-state, surface-energy-driven process. If our basic studies prove fruitful we may be able to develop a low temperature method, applicable to all crystalline film materials, for producing device-quality films on amorphous substrates. By means of lithography, defects in the films, such as dislocations and stacking faults, would be localized at predetermined positions out of the way of devices.

1.12 Ion-Beam-Enhanced Grain Growth in Thin Films

U.S. Air Force - Office of Scientific Research (Contract AFOSR-85-0154)
National Science Foundation (Grant ECS 85-06565)

Harry A. Atwater, Jerrold A. Floro, Henry I. Smith, and Carl V. Thompson

We have been investigating the effect of ion bombardment on the motion of grain boundaries in normal and secondary grain growth, so called ion-beam-enhanced grain growth (IBEGG). The scientific objective is to better understand how grain boundaries move. The technological objective is to develop a low temperature process for obtaining crystalline films on amorphous substrates. IBEGG has been studied experimentally in thin (i.e., < 1000 Å) Ge, Au and Si films. Ion beams in the 40 100 keV range have been employed, resulting in an ion damage profile with a peak approximately in the center of the thin film. Concurrent with ion bombardment, samples were annealed at 500 - 1050°C for Ge and Si, and at room temperature for Au. The temperature is chosen so that ion damage is annealed dynamically. IBEGG has been characterized by varying the ion dose, ion energy, ion flux, ion species, termperature, and thin film deposition conditions. The effect of these parameters on grain size and microstructure has been analyzed both qualitatively and quantitatively using transmission electron microscopy (TEM). A transition state model has been developed to describe the motion of grain boundaries during ion bombardment. The model accounts for the dependence of IBEGG on experimental parameters. An atomistic picture of the jump rate at grain boundaries

during IBEGG has been proposed. Monte-Carlo simulation of ion range and defect production was performed using the TRIM code and a modified Kinchin- Pease formula. The calculated defect yield per incident ion was correlated with enhanced grain growth and used to estimate the number of atomic jumps at the grain boundary per defect generated at the boundary for a given driving force, a quantity which is approximately constant for a given film material. The IBEGG and thermal growth rates have been related to their respective point defect population. That is, grain growth rate appears to depend only on the concentration of vacancies and interstitials, irrespective of whether they are created thermally or by ion bombardment.

1.13 Epitaxy via Surface-Energy-Driven Grain Growth

U.S. Air Force - Office of Scientific Research (Grant AFSOSR 85-0154)
Exxon Foundation

Joyce E. Palmer, Carl V. Thompson, Henry I. Smith

Grain Growth in polycrystalline films on single-crystal substrates can lead to formation of low-defect-density or single-crystal films. We are investigating surface-enery-driven secondary grain growth in silicon films deposited on a variety of insulating single-crystal substrates including CaF_2 and Al_2O_3. We are also further developing the theory of epitaxy by surface-energy-driven grain boundary motion.

1.14 Submicrometer-Period Gold Transmission Gratings for X-Ray Spectroscopy

Lawrence Livermore National Laboratory (Subcontract 9459005)

Erik H. Anderson, Mark L. Schattenburg,[2] Henry I. Smith

Gold transmission gratings with periods of 0.1 to 0.2 μ m, and thicknesses ranging from 0.5 to 1 μm are fabricated using x-ray lithography and electroplating. The x-ray masks are made either with holographic lithography or scanning-electron-beam lithography. Transmission gratings are either supported on polyimide membranes or are made self-supporting by the addition of crossing struts. They are used for spectroscopy of the x-ray emission from plasmas produced by high-power lasers. Gratings fabricated in our lab by these techniques are used in key diagnostic instruments associated with the soft x-ray laser research at Lawrence Livermore National Laboratory.

1.15 High-Dispersion, High-Efficiency Transmission Gratings for Astrophysical X-Ray Spectroscopy

National Aeronautics and Space Administration (Grant NGL22-009-683)

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[2] M.I.T. Center for Space Research

Eric H. Anderson, Mark L. Schattenburg, Claude R. Canizares[3], Henry I. Smith

Gold gratings with spatial periods of 0.1 - 10 μ m make excellent dispersers for high resolution x-ray spectroscopy of astrophysical sources in the 100 eV to 10 KeV band. These gratings are planned for use in the Advanced X-ray Astrophysics Facility (AXAF) which will be launched in the mid 1990's. In the region above 3 KeV, the requirements of high dispersion and high efficiency dictate the use of the finest period gratings with aspect ratios approaching 10:1. To achieve this we first expose a grating pattern in 1.5 μm thick PMMA over a gold plating base using Carbon-K x-ray nanolithography. To date, we have worked with gratings having periods of 0.3 or 0.2 μ m (linewidth 0.15 - 0.1 μm). Gold is then electroplated into the spaces of the PMMA to a thickness of 1 μm. Flight prototype gratings have been fabricated and are undergoing space worthiness tests. Efforts continue to increase the reliability and efficiency of the fabrication process.

1.16 Soft X-Ray Interferometer Gratings

Collaboration with KMS Fusion, Inc.

Erik H. Anderson, Henry I. Smith

In the soft x-ray region of the electromagnetic spectrum (1-10 nm) reliable optical constant data is scarce or non-existent. In order to fill this gap, an achromatic interferometer instrument is under construction at KMS Fusion, Inc. The critical optical components of this instrument are a set of matched, 200-nm-period transmission gratings which will be fabricated at M.I.T. Because these gratings will be used in an interferometer, the phase-front quality must be extremely good, and at the same time, the lines must be free-standing, i.e., have no support structure that would attenuate the x-rays. The fabrication process uses a thin membrane of silicon which is then etched to make free-standing lines. Gold lines were found to have too much distortion for this application.

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