Chapter 4. Nanostructures Technology, Research, and Applications

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4.1 NanoStructures Laboratory

The NanoStructures Laboratory (NSL) at MIT develops techniques for fabricating surface structures with feature sizes in the range from nanometers to micrometers and uses these structures in a variety of research projects. The NSL includes facilities for lithography (photo, interferometric, electron beam, and x-ray); etching (chemical, plasma and reactive-ion); liftoff; electroplating; sputter deposition and e-beam evaporation. Much of the equipment and nearly all the methods utilized in the NSL are developed in-house. Generally, commercial processing equipment, designed for the semiconductor industry, cannot achieve the resolution needed for nanofabrication, is inordinately expensive, and lacks the required flexibility.

The research projects within the NSL fall into three major categories: (1) development of submicron and nanometer fabrication technology, (2) short-channel semiconductor devices, quantum-effect electronics, and optoelectronics, and (3) periodic structures for x-ray optics, spectroscopy, atomic interferometry and nanometer metrology.

4.2 Scanning-Electron-Beam Lithography

Sponsor

Joint Services Electronics Program
Grant DAAH04-95-1-0038

Project Staff

Dr. James G. Goodberlet, Juan Ferrera, Mark K. Mondol, Professor Henry I. Smith

Figure 1 is a photograph of the scanning-electron-beam lithography (SEBL) system (VS-PL) located in Room 38-185. This instrument was obtained as a donation from IBM Corporation in November 1993. It is an experimental system based on many years of IBM technology development in SEBL. In 1994, a digital pattern generator was implemented, based on a commercial high-performance array processor, which utilizes dual RISC processors. In 1995, the capabilities of the pattern generator hardware were augmented. New shape primitives were incorporated into its software. Also, it is now possible to expose large mask designs composed of many stitched fields. Complementary to the pattern generator development was the implementation of conversion software, which allows a CAD data file to be fractured and translated prior to exposure by the electron-beam tool.

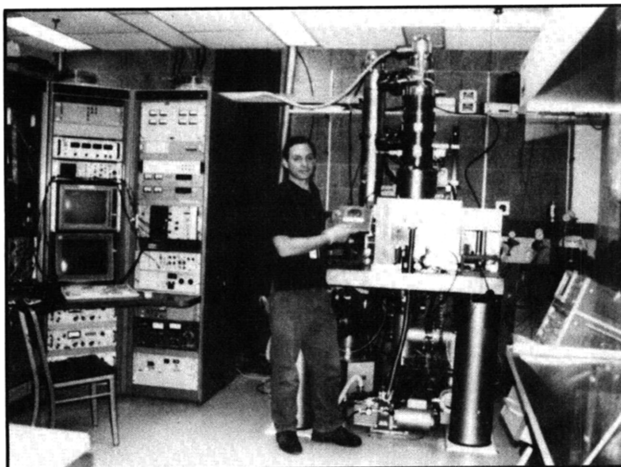

Figure 1. Photograph of the VS-PL scanning-electron-beam lithography system. The operator is Research Specialist Mark K. Mondol.

The VS-PL system is the cornerstone of a facility for high-performance electron-beam lithography at linewidth down to ~70 nm. The goals of the facility are to (1) provide the MIT research community with an in-house SEBL capability for writing directly on experimental device substrates, (2) advance the state-of-the-art in SEBL, particularly with regard to pattern placement accuracy and long-range spatial-phase coherence, and (3) pattern x-ray nanolithography masks for in-house use.

4.3 Spatial-Phase-Locked Electron-Beam Lithography

Sponsors

Joint Services Electronics Program
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Project Staff

Juan Ferrera, Dr. James G. Goodberlet, Mark K. Mondol, Professor Henry I. Smith

It is well known that scanning-electron-beam lithography can write extremely fine lines, ~10 nm in thin PMMA and ~1 nm in AlF_3. However, because writing fields in electron-beam (e-beam) lithography are quite small (~ 10^{14} beam steps), large-area patterns must be created by stitching together the small fields using a laser interferometer to provide X-Y positioning information. However, it is often overlooked that, due to instability, drift, and a variety of other problems, the precision with which this can be done is much poorer than the resolution. Typically, stitching errors of 30 to 100 nm are observed at field boundaries.

To solve this problem, we are developing a technology we call spatial-phase-locked electron-beam lithography (SPLEBL), which will provide pattern-placement accuracy and precision finer than the resolution, e.g., < 5 nm. The basic idea behind SPLEBL is to create on the substrate a spatially-coherent fiducial grid and to conduct all e-beam lithography with reference to it. The fiducial grid is produced by interferometric lithography (IL) to ensure long-range spatial-phase coherence.

We are developing two modes of implementation: the global fiducial grid and the segmented grid. In the latter approach, the grid is transferred onto the substrate only in small regions (2 x 2 μm square) at the corners of each e-beam scan field. Spatial-frequency-domain techniques are used to achieve sub-pixel alignment and scaling. In the global-fiducial-grid approach, the grid is transparent to the exposing e-beam and covers the entire top of the resist film while a pattern is being written. By collecting the emitted secondary electrons, or photons, a computer will keep track of the e-beam position at all times and correct for any drift or spurious displacement.

For the global-fiducial-grid mode of SPLEBL, we have developed a phase-locked loop (PLL), which has been modified for the e-beam application. In our PLL, phase, rather than frequency, is adjusted to lock the e-beam position to the spatial phase of the fiducial grid on the substrate. This circuit has been tested in scanning-electron-microscope (SEM) mode, as shown in figure 2. The images are of a 400 nm-period grating on the wafer. For the image obtained in figure 2a, the PLL was disconnected and a 60 Hz magnetic field was coupled to the e-beam column to provide an extreme form of disturbance. Without feedback, the 60 Hz field caused a 160 nm-amplitude periodic deflection of the e-beam. When the PLL was engaged, the 60 Hz disturbance was effectively canceled as shown in figure 2b. Additionally, the new PLL responds more quickly than the traditional PLL.

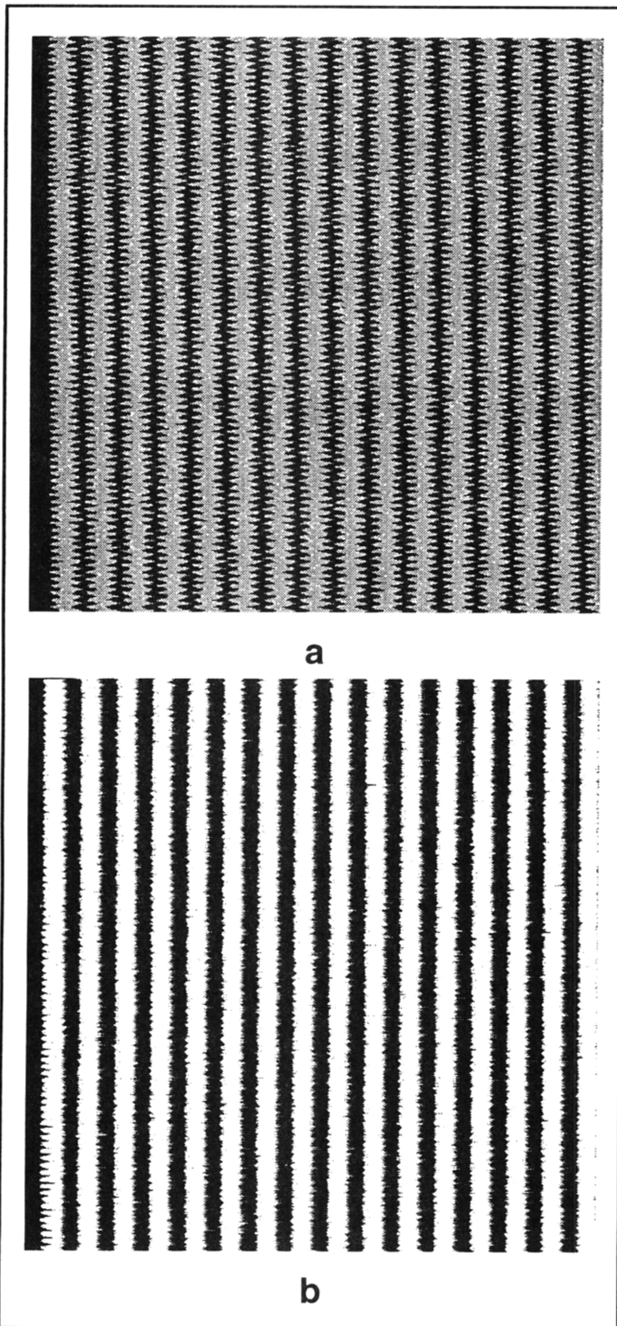

Figure 2. One-dimensional demonstration of spatial-phase locking using a 400 nm-period grating and a 60 Hz magnetic field to simulate a spurious disturbance. With the e-beam operating in SEM mode: (a) the 60 Hz field causes ~160 nm deflection of the electron beam; (b) with the phase-lock loop providing feedback, the disturbance is effectively canceled.

A one-dimensional lithographic experiment was carried out for the global-fiducial-grid mode of SPLEBL, in which the new PLL was used to write segments of 400 nm-period gratings in the corners of e-beam fields. The field size was 102 μm. Seventy-eight fields were stitched together, and the field stitching accuracy was evaluated by measuring spatial-phase discontinuities between gratings written in adjacent fields. An analysis of the data revealed a field-stitching accuracy of 3σ = 11 nm. This value compares well with results from a numerical simulation of the new PLL. The simulation, which uses contrast and signal-to-noise ratio values commensurate with those measured in the experiment, predicts a 3σ of 9 nm.

Results from the two modes of SPLEBL demonstrate that sub-10 nm stitching accuracies can be achieved in SEBL systems. SPLEBL has applications in x-ray and optical mask fabrication, and in development of optoelectronic devices, such as optical fibers for wavelength-division-multiplexed communications systems.

4.4 X-Ray Nanolithography

Sponsors

Defense Advanced Research Projects Agency/
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Project Staff

David J. Carter, James M. Carter, James M. Daley, Michael H. Lim, Euclid E. Moon, Mark R. Schweizer, Professor Henry I. Smith

For several years, we have been developing the tools and methods for x-ray nanolithography. We have explored the theoretical and practical limitations, and endeavored to make its various components (e.g., mask making, resists, electroplating, sources, alignment, etc.) reliable and "user friendly." Because of the critical importance of the x-ray mask technology, we discuss this in a separate section, 4.5.

Our sources for x-ray nanolithography are simple, low-cost electron-bombardment targets, typically Cu_L (λ = 1.32 nm), separated by a 1.4 μm-thick SiN_x vacuum windows from helium-filled exposure chambers. In the future, we hope to replace Cu_L sources with higher flux sources.

For applications such as CMOS and T-gate GaAs devices, which require alignment of two or more levels of lithography, we have developed a high-precision mask alignment and gapping system (see section 4.6). For most other applications, including quantum-effect devices, alignment is not critical, and a single level of exposure is all that is required.

In earlier research, we showed that for wavelengths longer than 0.8 nm, the important limitation on resolution is diffraction in the gap between mask and substrate. Figure 3 summarizes this, which is the result of extensive simulations of the diffraction field, taking into account the vectorial nature of the electromagnetic radiation, the dielectric properties of the absorber, and the spatial incoherence of the source. At α = 1, the process latitude is very wide, and all feature types print within 10 percent of the dimensions on the mask. At α = 1.5, latitude is smaller and features print well, but some require biasing on the mask. At α > 2, significant diffraction occurs, requiring modeling of the aerial image to determine the mask structure necessary to achieve a desired image.

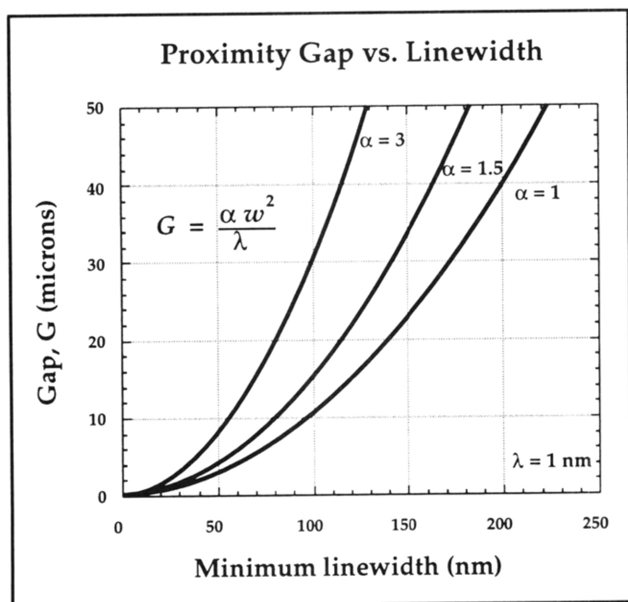

Figure 3. Plot of the minimum feature size versus mask-sample gap, G, at λ = 1 nm, for three values of the parameter α.

As indicated in figure 3, for replicating features below about 70 nm, the mask-sample gap must be below 5 μm. For such high resolution work, we use soft contact. That is, since the mask is a compliant membrane only 1 μm thick, one can bring the mask into contact with the substrate without causing any damage. We use both electrostatic means and partial vacuum to effect this soft contact.

A scanning-electron-beam lithography system is used to write an x-ray mask, as illustrated in figure 4. Features as fine as 25 nm are achieved in this step using the e-beam system at the Naval Research Laboratory (NRL). This pattern is plated up in gold and then a replica, or "daughter mask," is created using soft-contact x-ray nanolithography and electroplating. Finally, in the case shown by AuPd liftoff, this daughter mask is exposed on a device substrate, and the pattern is transferred.

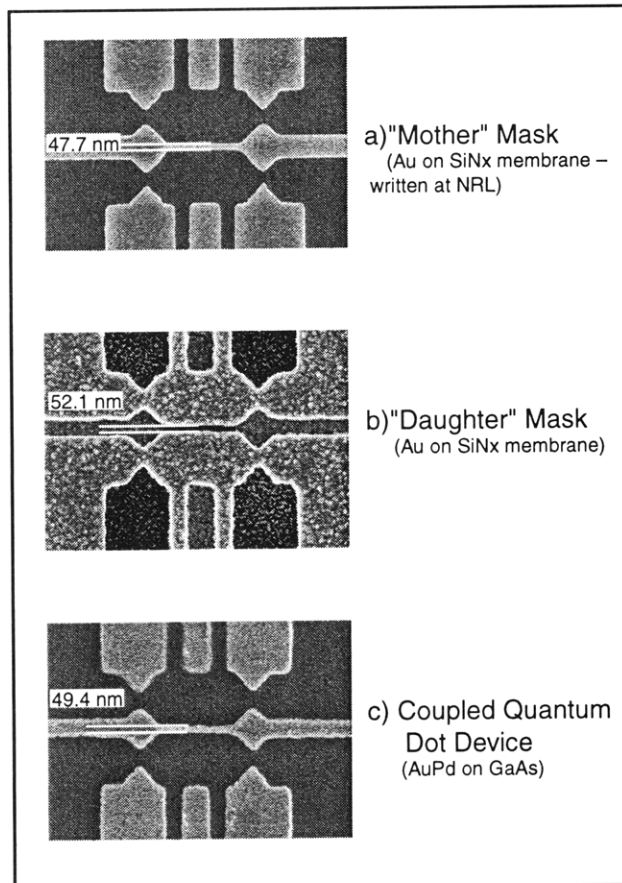

Figure 4. Scanning-electron micrograph illustrating three stages of soft-contact x-ray nanolithography. (a) The "mother" x-ray mask, a pattern in electroplated gold on a 1-micron-thick SiN_x membrane formed subsequent to exposure with scanning-electron-beam lithography (at the Naval Research Laboratory (NRL)). (b) Replication using 1.3 nm x-rays, of the mother mask onto another x-ray mask, the "daughter," and electroplating in gold. This step reverses the "polarity." (c) Replication of the daughter x-ray mask onto a GaAs substrate; the device is a coupled pair of quantum-dot single-electron transistors.

Figure 5 illustrates that 25 nm features are achievable today with 1.3 nm soft-contact x-ray nanolithography and electroplating pattern transfer.

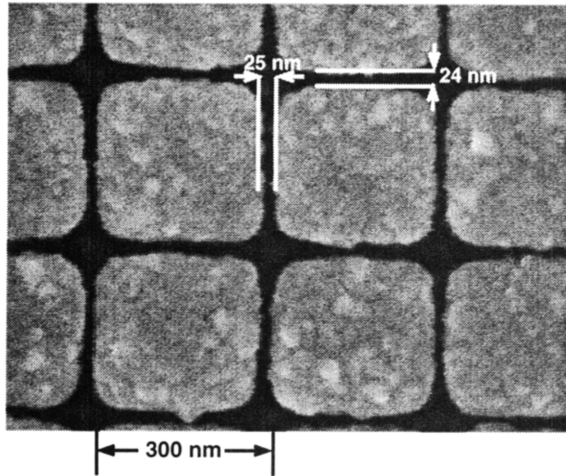

Figure 5. Scanning-electron micrograph illustrating that 25 nm features are achievable using 1.3 nm soft-contact x-ray nanolithography followed by gold electroplating. The mother x-ray mask was written at NRL and contains the patterns for a family of lateral-surface-superlattice devices.

Soft-contact x-ray nanolithography is unique to MIT and although suitable for research it is considered incompatible with manufacturing. Accordingly we have sought an alternative approach that would preserve the desirable features of x-ray lithography with 1.3 and 4.5 nm photons while circumventing the need to bring the mask into intimate contact with the substrate. Our proposed solution is illustrated in figure 6, a maskless projection lithography system that employs an array of Fresnel zone plates.

As illustrated, an array of Fresnel zone plates focuses an incident beam of 4.5 nm x-rays from a microundulator forming an array of spots on a substrate. Writing is done via a dot-matrix-printing strategy, with the individual beams multiplexed by an array of grazing-incidence micromechanical mirrors located upstream of the zone-plate array. Registration of the writing will be done continuously under laser interferometer control. Fresnel zone plates can focus 4.5 nm x-rays with 31 percent efficiency. The resolution or spot size is approximately equal to the width of the outermost zone. Hence, the resolution of the figure 6 system is determined by one's ability to make the zone plates by e-beam lithography and dry etching.

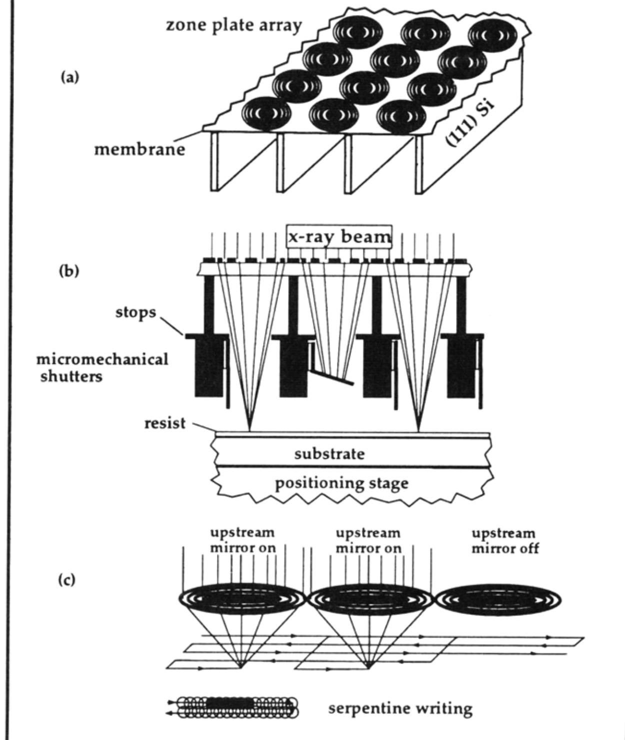

Figure 6. Schematic of a maskless projection lithography scheme that employs 4.5 nm x-rays and hence should be capable of sub-25 nm lithography. The zone plates focus 4.5 nm x-rays with 31 percent efficiency. Writing is done via a dot-matrix strategy using laser interferometry to ensure precise registration. Although (b) depicts multiplexing of individual beamlets by micromechanical shutters, in practice this will most likely be done by upstream grazing-incidence micromechanical mirrors (c).

The maskless projection system, shown in figure 6, should have none of the problems associated with masks, such as distortion, defects, and slow turnaround. Moreover, because of the low energy of the 4.5 nm photon (280 eV) there will be negligible substrate damage, and no deleterious backscattering or proximity effects.

4.5 Improved Mask Technology for X-Ray Lithography

Sponsors

Defense Advanced Research Projects Agency/
Naval Air Systems Command
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Joint Service Electronics Program
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Project Staff

James M. Carter, James M. Daley, Michael H. Lim, Wendy Mao, Mark K. Mondol, Edward R. Murphy, Isabel Y. Yang, Jing Yuan, Professor Henry I. Smith

At feature sizes of 100 nm and below the mask-to-sample gap, G, must be less than ~10 μm (see figure 3). We have developed a mask configuration compatible with this requirement in which the mask membrane is flat to ~100 nm. A novel, low-gradient furnace was developed to achieve such high a level of mask flatness.

Our mask technology is based on low-stress, Si-rich silicon nitride, SiN_x. This material is produced in the Integrated Circuits (IC) Laboratory at MIT in a vertical LPCVD reactor. Membranes of SiN_x can be cleaned and processed in conventional stations. Radiation hardness remains a problem at dose levels corresponding to production (i.e., millions of exposures). For research purposes, however, the material is acceptable.

For absorber patterns, we use both gold, Au, and tungsten, W. The gold is electroplated onto the membrane after resist exposure and development using a specially designed apparatus. The stress of the gold, which affects the in-plane distortion, is controlled via the plating conditions. The W is sputter deposited and patterned by reactive-ion etching. In order to ensure uniform W stress over an entire membrane, a He-backside temperature-homogenization apparatus was developed. Recently, we have begun to investigate amorphous alloys of tantalum, such as Ta_3B. These alloys tend to provide excellent linewidth control and stability with time. Moreover, they can be annealed to produce near-zero stress.

For periodic structures, patterning of x-ray masks is done by interferometric lithography (IL), but for patterns of arbitrary geometry, it is done by e-beam lithography, either in the MIT e-beam facility or in collaboration with NRL or IBM. We use CAD tools at MIT and convert the data into formats compatible with the e-beam exposure systems. Data is shipped to NRL or IBM over the internet. After e-beam exposure, masks are shipped back to MIT by express mail where development and Au electroplating are carried out. This collaboration has already demonstrated that patterning x-ray masks by e-beam can be done remotely.

The Digital Instruments STM/AFM was found to be highly effective in inspecting x-ray masks, providing information on defects not apparent by other means.

For etching W absorber patterns on x-ray masks, a reactive-ion-etching process is required, which puts considerable power into the membrane substrate. Since membranes have very low thermal mass and conductivity, we use He-backside cooling in a reactive ion etcher. Membranes can be cooled to below -20 degrees C. At such low temperatures, the isotropic etching component is suppressed leading to highly directional etching.

Figure 7 illustrates a new concept for fabricating x-ray masks that we are developing which should be especially valuable for gaps less than 15 μm. In brief, after creation of the absorber pattern on the membrane, the latter is bonded anodically to the mesa rim of a Pyrex frame. In this way, the critical absorber pattern can be protected within a He-filled enclosure from the accumulation of dust, as depicted in figure 8. Dust and contamination that might accumulate on the 1 μm-thick mask membrane can be removed by aggressive methods including brushing. The x-ray-transparent pellicle on the back side of the glass frame could be made of, for example, 250 nm-thick SiN_x. It would not need to be cleaned aggressively since dust particles on it would not be imaged on the substrate due to diffraction and penumbral blurring. Figure 9 illustrates that the membranes bonded according to figure 7 are extremely flat, ~100 nm. The figure 8 mask configuration also includes an edge reinforcement which provides a transition from the rigid mesa to the membrane.

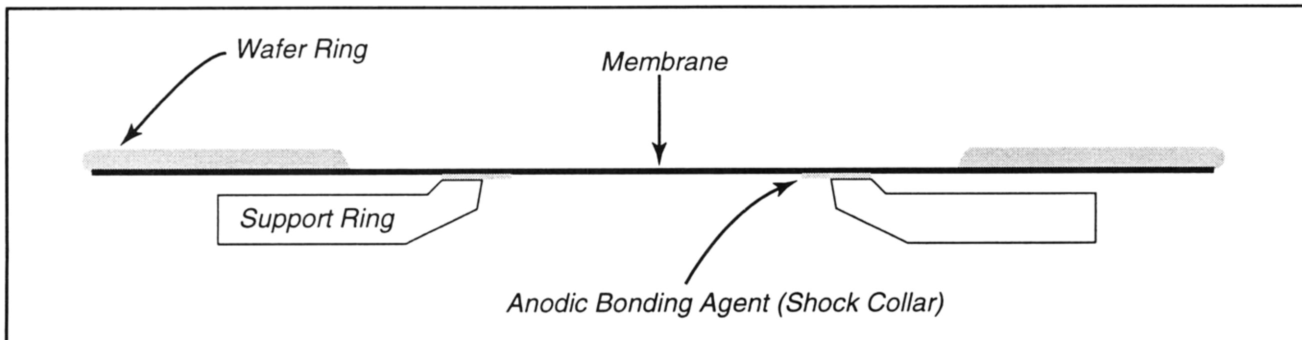

Figure 7. To achieve the protection of the absorber pattern depicted in figure 8, the mask's membrane is anodically bonded to the mesa rim of the Pyrex frame after formation of the absorber pattern.

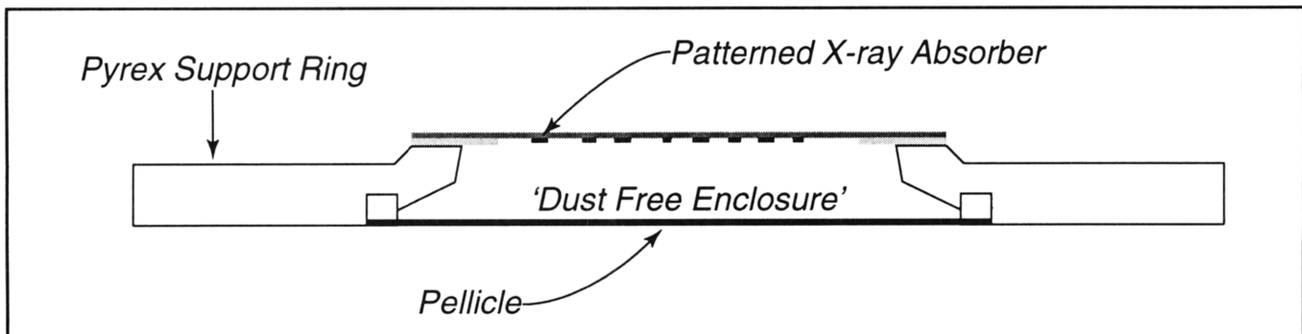

Figure 8. Schematic showing how the absorber pattern on an x-ray mask can be protected from the accumulation of dust and other contamination by enclosing it between the membrane and a pellicle. The mask is also provided with an edge reinforcement to eliminate the abrupt transition from rigid mesa to membrane, thereby reducing the chance of breakage. In this configuration, dust accumulated on the membrane can be removed by aggressive techniques.

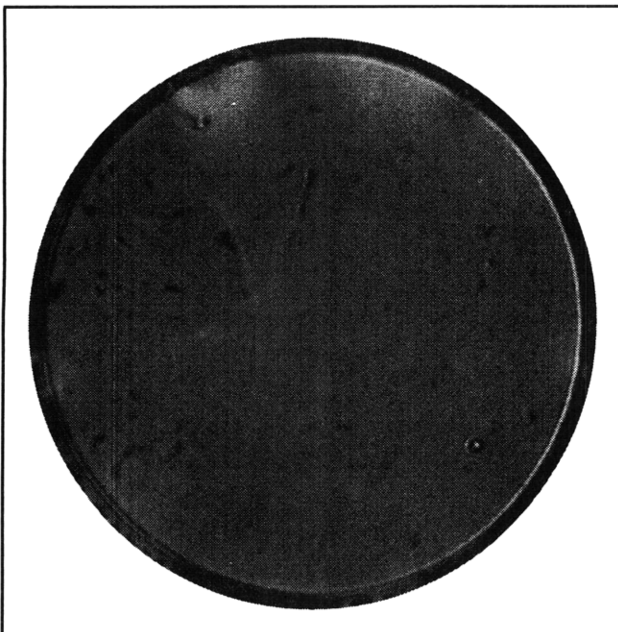

Figure 9. Interferogram of the top surface of an x-ray mask membrane bonded to a Pyrex frame as in figures 8 and 9. The deviation from perfect flatness is undetectable except in one spot where it is about 100 nm.

4.6 A High-Precision Mask Alignment and Gapping System with Immunity to Overlayers

Sponsors

Defense Advanced Research Projects Agency/
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Contract N00019-95-K-0131
Joint Services Electronics Program
Grant DAAH04-95-1-0038

Project Staff

Dr. Patrick N. Everett, Euclid E. Moon, Professor Henry I. Smith

A high-precision mask alignment and x-ray exposure system (figure 10) was constructed and incorporates our novel interferometric broad-band imaging (IBBI) alignment technique. This scheme employs grating and grid type alignment marks on mask and substrate, respectively, which are viewed through the mask from outside the x-ray beam at a Littrow angle with f/10 optics and a 110 nm working

Figure 10. Mask-wafer alignment and x-ray exposure system.

distance (figure 11). The viewing/illuminating optics are positioned in a plane parallel to the grating lines, resulting in symmetric higher-order diffraction by the mask and wafer. Each mark consists of two gratings (or grids) of similar periods, arranged so that only dissimilar periods are superimposed during alignment. Using a CCD camera, misalignment is measured from two identical sets of moiré fringes (~50 micron period) that move in opposite directions as the mask is moved relative to the substrate. Alignment corresponds to matching the spatial phases of the two sets of fringes.

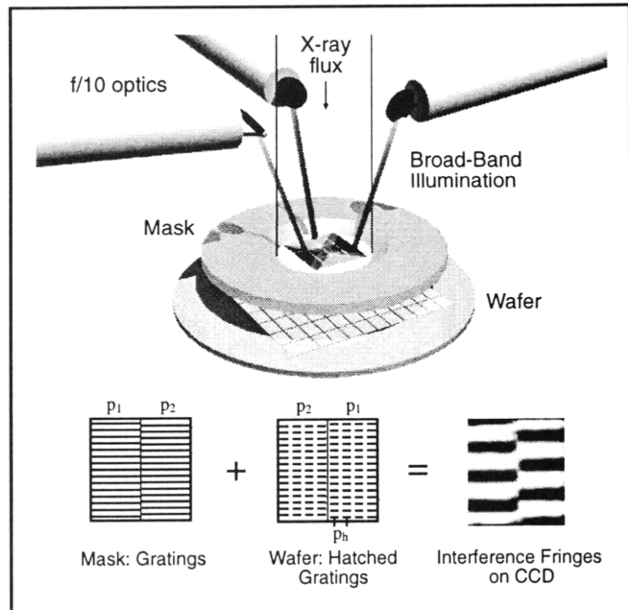

Figure 11. Interferometric broad-band imaging scheme. Alignment is signified by relative spatial phase of counter-moving interference fringes.

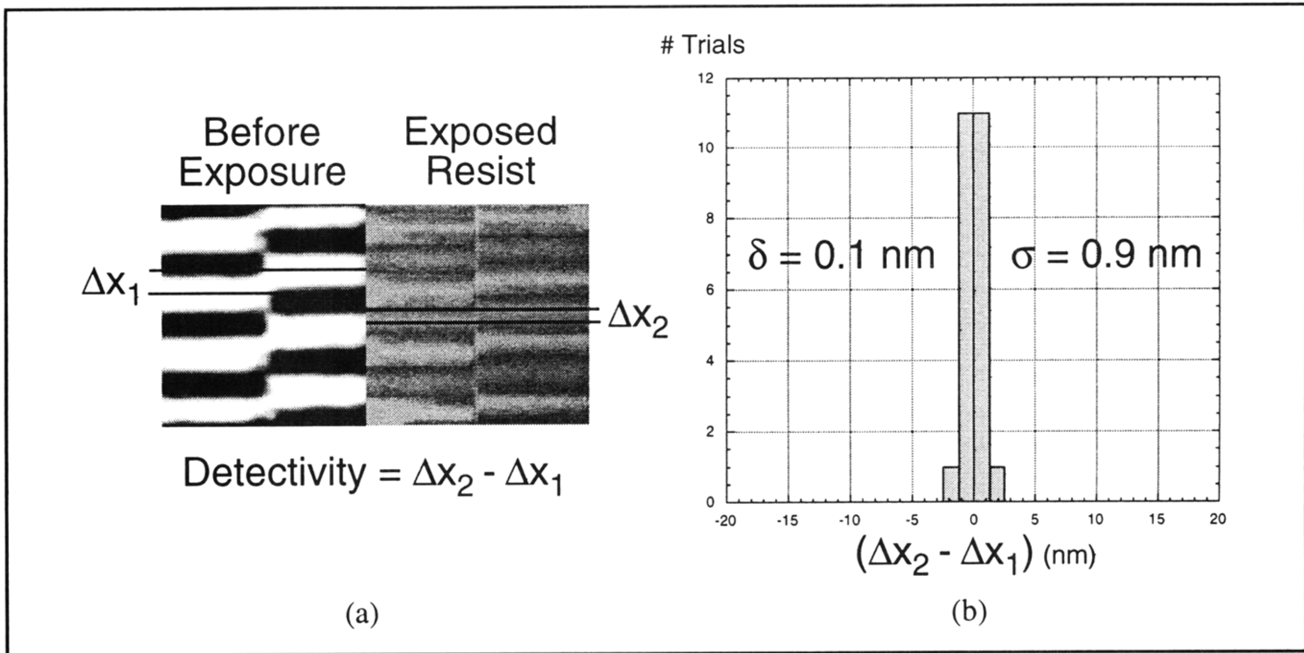

Figure 12. (a) Interference fringes as detected by IBBI optics compared with moiré fringes in exposed resist on patterned wafer; (b) Statistics of the difference of these measurements.

For our in-house device fabrication, the combination of the high-detectivity of IBBI (σ = 0.9 nm) and the high-repeatability of the closed-loop piezo mask stage (σ = 2 nm) is expected to satisfy alignment requirements for device features down to 20 nm. The IBBI alignment technology presently is being transferred to a commercial manufacturer for use in their next-generation of x-ray lithography steppers.

To determine the detectivity of IBBI, a comparison was made between: (1) alignment of a mask and wafer as seen by the IBBI optics, and (2) alignment of the exposed pattern at zero gap with a first-level pattern (figure 12a). Since the theoretical detectivity of IBBI (~0.5 nm) is higher than conventional metrology tools, we determined pattern placement by observing moiré fringes (using an ordinary bench microscope) between an alignment mark exposed in resist and an alignment mark previously etched into a wafer. The spatial-phase differences corresponding to alignment offsets were determined in both cases with frequency-domain image analysis. Statistics for alignment marks of 1 micron period (figure 12b) illustrate that our implementation is close to the theoretical maximum detectivity.

To ensure linewidth control, one must detect gap with high precision. We have devised a gapping scheme that uses a mask alignment mark as a beam splitter, with two arms of the interferometer being the mask thickness and the mask-wafer gap (figure 13). Illuminating the mask mark with polychromatic light results in an intensity variation as a function of gap. During a limited scan of gap, a beat pattern is obtained on each side of the mark, where the beat periods are determined by the periods of the gratings. Comparing these beat patterns yields an unambiguous measure of gap, with a sensitivity of less that 50 nm.

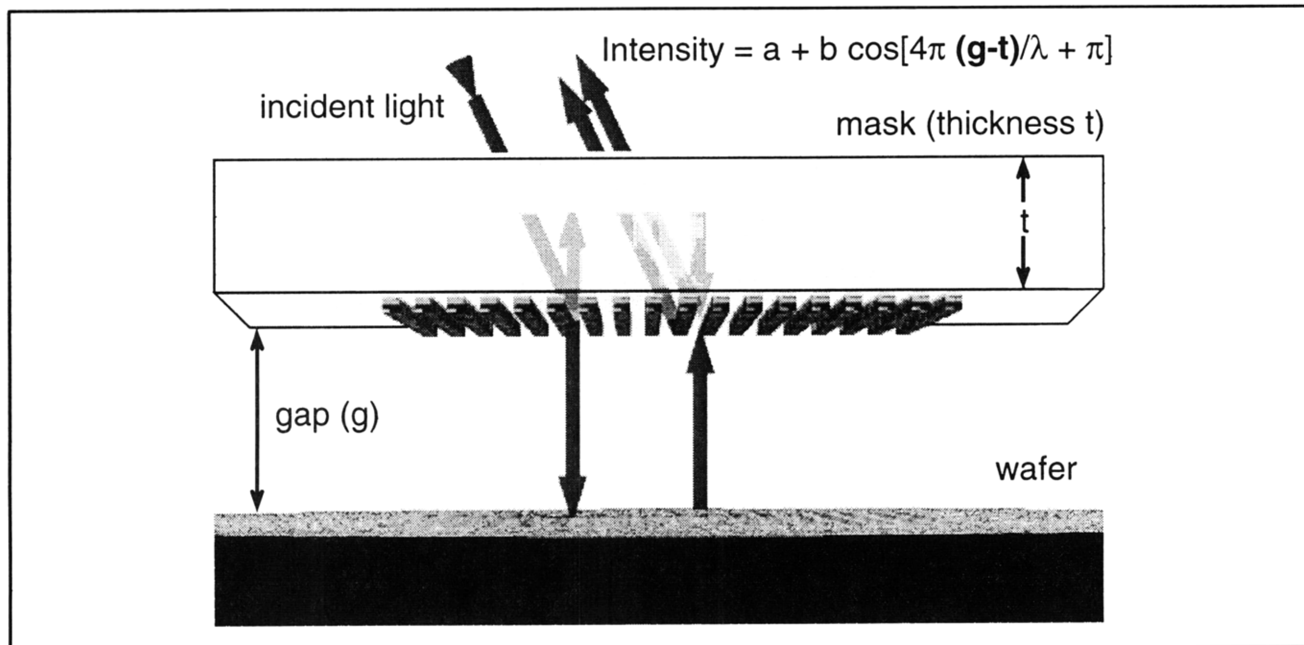

Figure 13. Gapping with diffractive Micheson interferometer.

4.7 Interferometric Lithography

Sponsors

Joint Services Electronics Program
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Project Staff

James M. Carter, Maya S. Farhoud, Juan Ferrera, Robert C. Fleming, Timothy A. Savas, Dr. Mark L. Schattenburg, Professor Henry I. Smith

Interferometric (also called holographic) lithography schemes are preferred for the fabrication of periodic and quasi-periodic patterns that must be spatially coherent over large areas and free of phase errors. For spatial periods down to 200 nm, an argon ion laser is used in a Mach-Zehnder configuration with a unique fringe-locking feedback system. This produces large area (10-cm diameter) gratings with long-range spatial-phase coherence, free of phase errors or detectable distortion. The fringe locking ensures reproducibility of exposure.

Interferometrically produced gratings and grids are used as fiducials in spatial-phase locked electron-beam lithography in order to achieve pattern placement accuracy in the nanometer range. This application requires the fiducial to be characterized with precision equal or better than the pattern placement desired. A direct measurement of the phase fidelity of interferometric gratings has been implemented. To ensure freedom from distortion, the gratings are exposed by combining spherical waves, which emanate from spatial filters, at the substrate plane. Therefore, the grating has a non-linear phase progression which can be modeled by means of a simple mathematical model that assumes the spatial filters to be point sources. To confirm the validity of this model, we use a self-reference technique which measures the difference in phase between two gratings exposed in the same system, displaced from each other by a known amount. The small non linearity in the gratings' phase progression results in a macroscopic beat pattern, or moiré. The phase difference between the gratings is then measured by a method akin to phase shifting-interferometry. Figure 14 shows the result of such a measurement. The measured values are then compared to the theoretical prediction. At the present time, the accuracy of these measurements is estimated to be on the order of 50 nm. The gratings exhibit no distortions at this scale. Further improvements will enable us to characterize interferometric gratings with a higher degree of phase-error detectivity.

For spatial periods below 200 nm, bright light sources, with wavelengths below 200 nm, must be used. Such sources have limited temporal coherence, thus one must employ an achromatic scheme such as shown in figure 15. The source is an ArF laser (193 nm wavelength). A collimating lens, polarizer and scanning system are interposed between the source and the interferometer in order to achieve reasonable depth-of-focus and large

exposure areas. We also use a white light interference principle to ensure equal path lengths in the two interferometer arms. Using this system, gratings and grids of 100 nm period (nominally 50 nm lines or posts) are obtained in PMMA on top of a specially designed antireflection coating. Figure 16 shows a 100 nm-period grid etched into Si following achromatic interferometric lithography.

Grids such as shown in figure 16 are of interest in a number of applications including high-density magnetic information storage, and flat-panel displays based on field emission. At present we use interferometric lithography to produce grid exposures of 200 and 320 nm period for a flat-panel-display program at MIT Lincoln Laboratory. In the future, we expect to provide similar grids for Professor Akinwande who also conducts research on flat-panel displays.

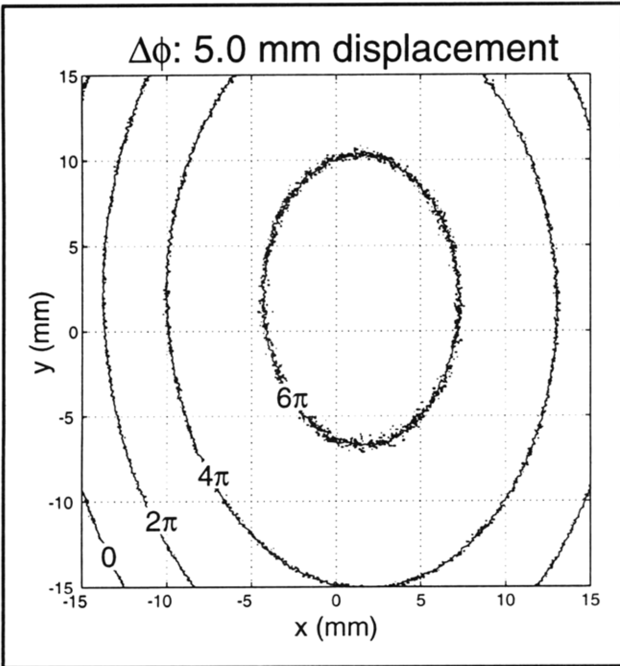

Figure 14. Plots of phase difference between two identical, laterally displaced 400 nm period gratings, measured by means of the phase-shifting moiré technique. Contours of constant phase are plotted. The two gratings are displaced by 5.0 μm.

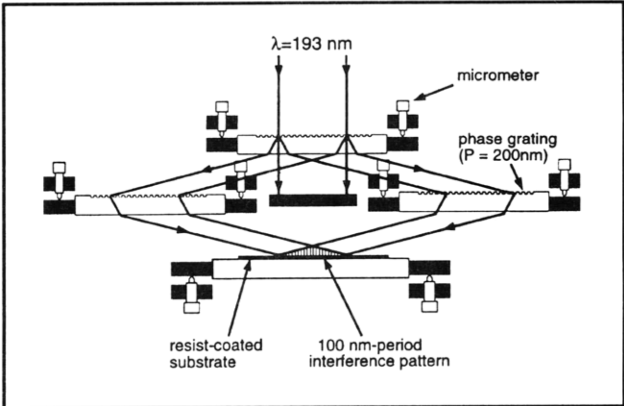

Figure 15. Achromatic interferometric lithography (AIL) configuration.

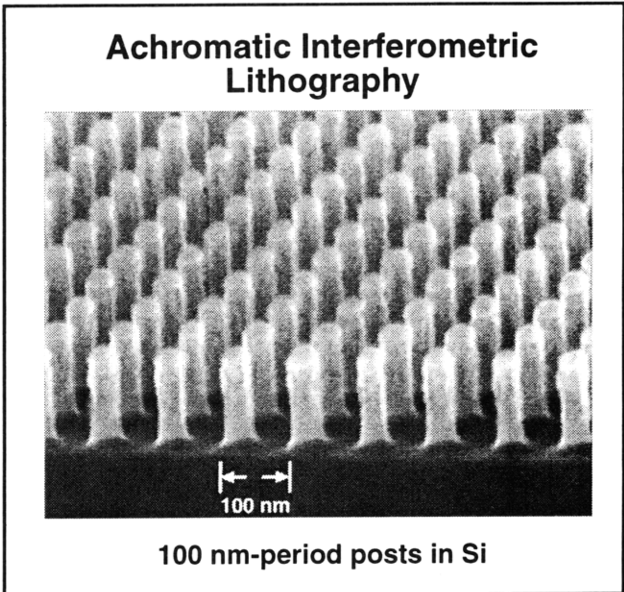

Figure 16. Scanning electron micrograph of a 100 nm period grid, exposed in PMMA on top of specially designed antireflection coating and transferred into Si by reactive ion etching.

4.8 High-Performance Sub-100 nm MOSFETs using X-ray Lithography

Sponsors

Defense Advanced Research Projects Agency/
Naval Air Systems Command
Contract N00019-95-K-0131
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Joint Services Electronics Program
Contract DAAH04-95-1-0038
National Science Foundation
Graduate Fellowship
U.S. Navy - Office of Naval Research
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As MOSFET dimensions are scaled to lengths below 100 nm, major challenges arise in the design and fabrication of devices. Our efforts have leveraged off the ability of x-ray lithography to easily print linewidths in this range, thus providing us with the ability to work on design issues at the limits of MOSFET scaling.

Current fabrication efforts are focused on making a new x-ray mask for defining the gate level of a new set of MOSFETs. The mask fabrication technology mixes and matches the optical stepper to the e-beam tool. Coarse patterns, such as pads and e-beam-field-alignment marks, are first transferred onto a chrome coated quartz wafer using the optical stepper. This wafer becomes a mask which is used to make a one-to-one pattern transfer of the coarse features onto the x-ray mask using proximity 240 nm-UV exposure. The coarse patterns and the field alignment marks are plated up in gold and sent to the e-beam for fine pattern writing, see figure 17. Using this process, significant e-beam time is saved since the coarse features do not need to be written. In addition, field-alignment marks ensure that the features written by the e-beam overlay properly with features exposed by optical projection lithography. We have calibrated our e-beam lithography system to write line widths from 60 nm to 300 nm reproducibly. The new gate-level mask written with this process will be used in the x-ray lithography step that defines the gate level of a new set of NMOS devices in bulk silicon with L_{eff} below 70 nm. The design of these devices, building upon our previous success in fabricating robust 100 nm NMOS, will focus on exploring the optimization of source and drain design for devices in this size range. Along with making working devices at such short lengths, we hope to gain insight into the critical pieces of source drain design for sub-100 nm devices.

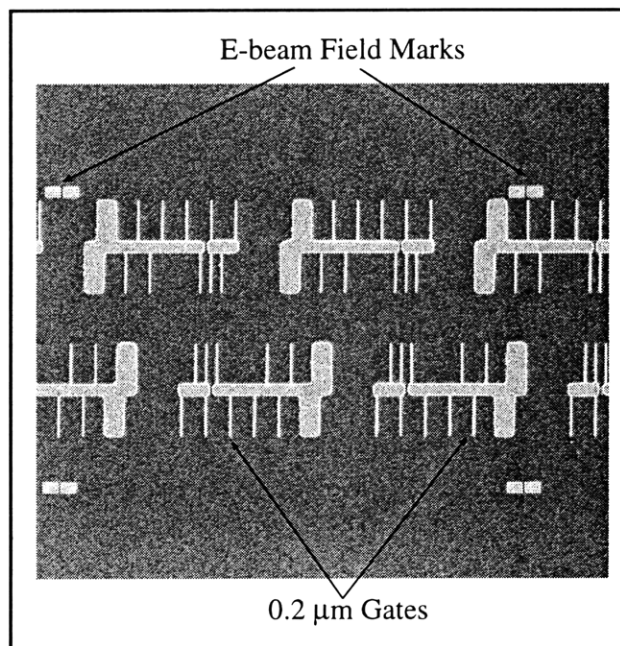

Figure 17. Scanning electron micrograph of a portion of an x-ray mask patterned with the VS-PL e-beam system, showing the gate level for deep-submicron silicon-on-insulator devices.

Another avenue for improved MOSFET performance is the reduction of operating temperature. Our measurements show that at 80 K the devices turn on and off more sharply (the subthreshold slope improves from 80 to 24 mV/decade) and transconductances are at least 50 percent higher, see figure 18. Such advantages provide another scaling option which may allow future devices to surpass the limits seen for room temperature operation. With the new set of shorter devices, we will explore the advantages and optimization of cryogenic temperature operation of sub-100 nm channel length devices.

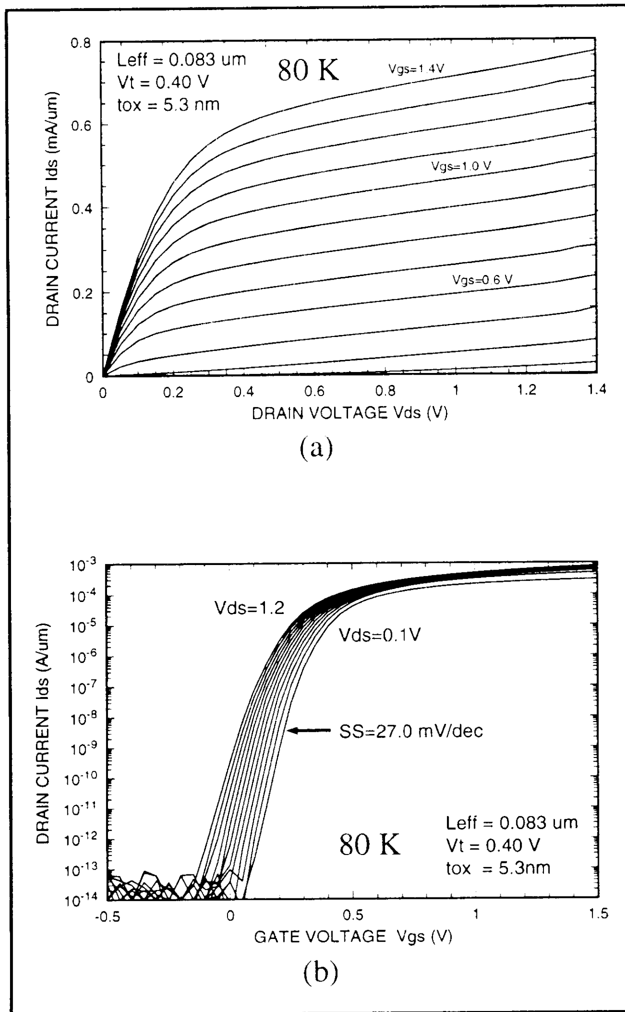

Figure 18. I-V characteristics of an 83 nm-channel-length NMOSFET cooled to 80 K.

4.9 Back-gated CMOS on SOI Active Substrates

Sponsors

Defense Advanced Research Projects Agency/
Naval Air Systems Command
Contract N00019-95-K-0131
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Contract 1622
Joint Services Electronics Program
Contract DAAH04-95-1-0038
National Science Foundation
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Project Staff

Anthony Lochtefeld, Isabel Y. Yang, Professor Dimitri A. Antoniadis, Professor Anantha P. Chandrakasan, Professor Henry I. Smith

The merits of conventional fully-depleted CMOS on silicon-on-insulator substrates (SOI) such as near-ideal subthreshold slope at low-threshold voltages, and low-junction capacitance with simple isolation scheme has qualified this technology to be a promising candidate for low-power systems. To further exploit the advantages of fully-depleted SOI for ultra-low-power and high-performance applications, we have developed a new technology, SOI on active substrate (SOIAS). This technology involves the formation of a back-gated SOI device where the back-gate is formed by burying a conductive layer underneath the buried oxide and contacting it from above. Figure 19 shows the cross section of such a device structure. The purpose of the back-gate is to dynamically control the threshold voltage of the normal transistor on top. This approach addresses the opposing requirements of high performance and low power, particularly at low-power supply voltages (e.g., 1.5 V or less). Power dissipation management in such a scheme can be accomplished by selectively lowering the threshold voltage when a circuit is active, and raising the threshold voltage when the circuit is idling to reduce static leakage. Power savings can be dramatic in circuits which are idling most of the time.

The SOIAS substrate is a multilayered blanket film stack consisting of the silicon wafer, oxide, intrinsic polysilicon, back-gate oxide, and silicon film. These substrates were prepared using either bonded SIMOX or etched-back bulk wafers. For the bonded SIMOX process, the back-gate oxide-to-be was formed by dry oxidation, and intrinsic amorphous silicon was deposited as the back-gate-to-be material on the device wafer. This device wafer was then flipped and bonded to a thermally oxidized handle wafer, and annealed. The bonded wafers were then etched to remove the bulk of the SIMOX wafer, stopping on the buried oxide. Therefore, the resulting silicon film thickness is as uniform as that of the original SIMOX wafer. The bulk bonding and etch-back process is similar to the SIMOX process except that the device wafer is thinned down by chemical/mechanical polishing.

Device fabrication on SOIAS substrates follows the conventional CMOS SOI process with two additional steps. N+ and P+ back-gates are formed via implantation through the silicon film in two masking steps. By properly tailoring the energy and dose of the implant, the back-gate and V_T-adjust implants can be done in one step. Using the same type of doping in the back-gate poly and silicon film results

in near-zero flatband voltage at the back-gate. The front-gate device is then built as in a conventional SOI CMOS process using LOCOS isolation with an additional step of cutting the back-gate contacts. An alternative process currently under development utilizes back-gate patterning prior to bonding, allowing dielectric isolation between the back-gates (as shown in figure 19) and minimum back-gate dimensions. This will reduce the capacitance between back-gate and source or drain. In addition, higher doping and silicidation of the back-gates will be possible for low resistance. Figure 20 is a scanning-electron micrograph of the SOIAS device. Figure 21 shows the measured I-V characteristics of a NMOS device, demonstrating the effects of electronically controlling the V_T on leakage current. A 250 mV change in threshold voltage results in a four decade reduction in off current and a 80 percent current increase at 1 V operation.

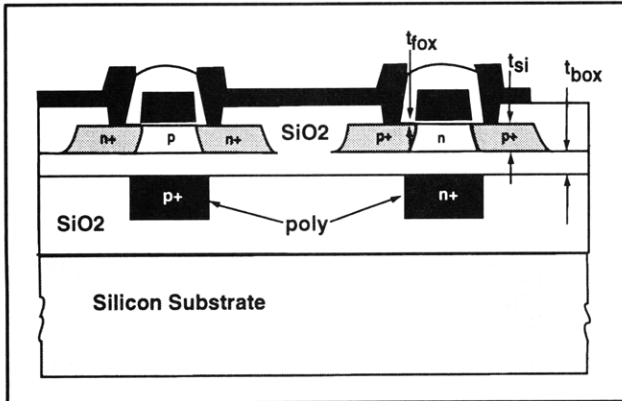

Figure 19. SOIAS back-gated CMOS device schematic.

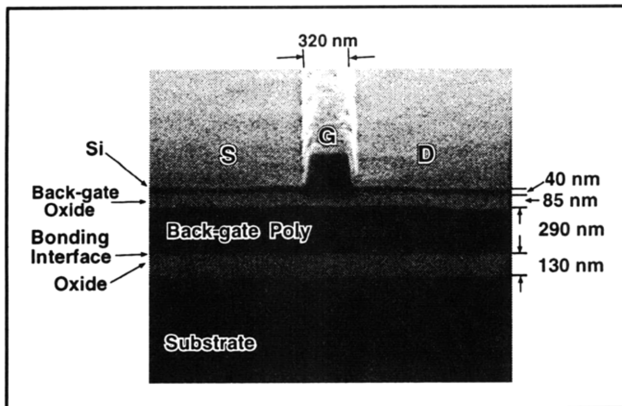

Figure 20. SEM micrograph of SOIAS device cross-section.

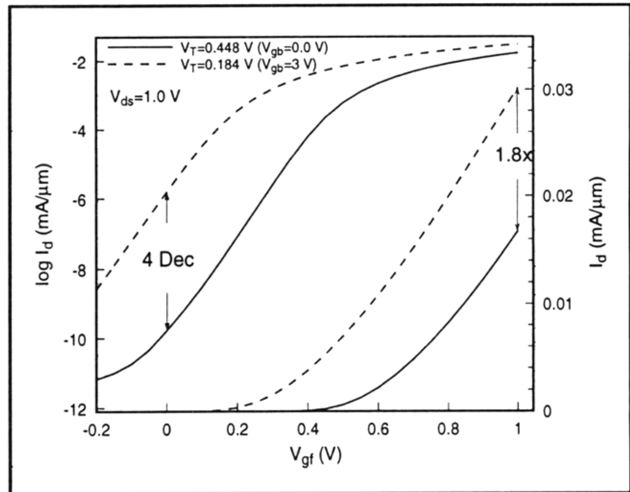

Figure 21. NMOS subthreshold characteristics.

We have taken advantage of the SOIAS technology to investigate the SOI CMOS ultra-low power design space. Independent access to NMOS and PMOS back-gates allows measurements for a range of V_T and V_{DD} operating conditions using the same set of devices; hence, all measured quantities are self-consistent. Figure 22 shows the measured total energy for a 101-stage inverter ring oscillator running at three different frequencies, indicating that an optimal V_T exists for minimum power for a given V_{DD}. Below this V_T, here around 250 mV, increase in static power dissipation offsets the reduction in dynamic (switching) energy. Figure 23a-c demonstrates the effects of varying V_{DD} and V_T on static and dynamic energy dissapation, and propagation delay. The delay per stage was obtained from 101-stage inverter ring oscillators, and the dynamic and static leakage currents were measured on identical inverter chains.

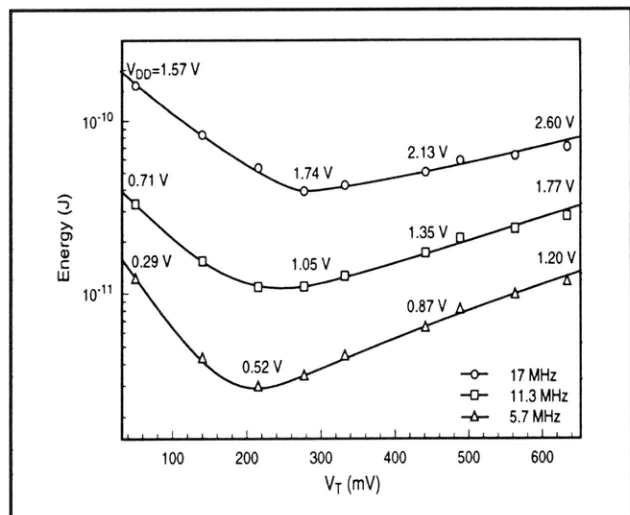

Figure 22. Measured total energy for 101-stage ring oscillator.

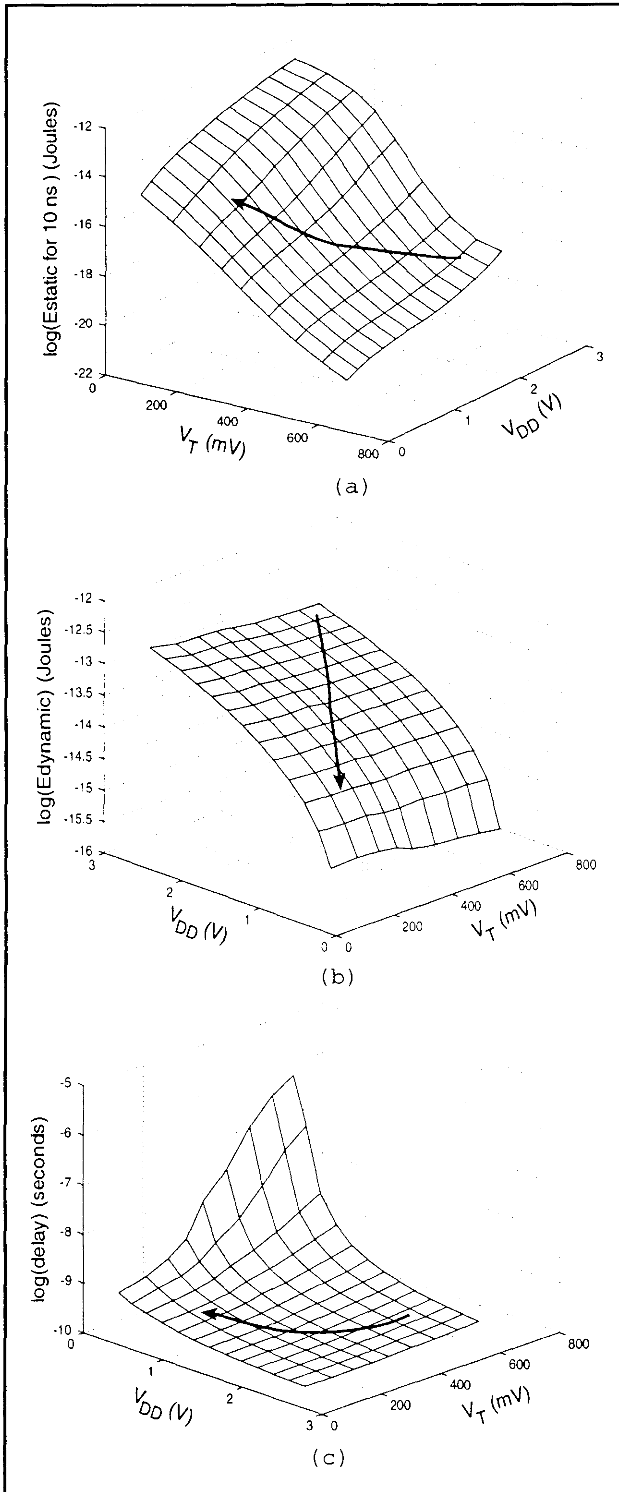

Figure 23. Measured static (a), and dynamic (b) energies, and delay perstage (c) as a function of V_T and V_{DD}.

We have developed an energy consumption model for SOIAS, taking into account front- and back-gate switching energies and static leakage energy. By using the measured switching and static leakage energies with the energy consumption model, the optimal V_{DD} and V_T can be found for different system activities with dynamic switching of the V_T. The switch in the V_T was 250 mV. Module and back-gate activity factors were obtained from profiling of a SPEC benchmark program, assuming burst mode operation (1 percent module activity, in this case) and a clock frequency of 100 MHz. Figure 24 compares the optimal V_T, V_{DD} and energy for constant and dynamic switching of the V_T. Dynamic switching of the V_T allows reduction of optimal V_T and V_{DD} without suffering from high static leakage energy, providing significant energy savings while maintaining the same performance.

	Optimal V_T (mV)	Optimal V_{DD} (V)	Normalized Total Energy
Const. V_T Adder	277	0.59	1
Var. V_T Adder	51	0.26	0.21
Const. V_T Shifter	413	0.81	1
Var. V_T Shifter	139	0.37	0.23
Const. V_T Mult.	629	1.15	1
Var. V_T Mult.	333	0.69	0.4

Figure 24. Optimal V_T and V_{DD} at minimum total energy for several functions modules.

4.10 Fabrication of T-gate Devices Using X-ray Lithography

Sponsor

U.S. Army Research Office
Contract DAAH04-94-G-0377

Project Staff

Mitchell W. Meinhold, Professor Henry I. Smith

Monolithic microwave integrated circuits (MMICs) have potential applications in automobile navigation, collision-avoidance, and wireless communication systems. The high-speed MODFET devices of such circuits require very short gate lengths, while preserving low resistance. Large gate widths are required for high current drive. To meet these conflicting demands, so-called "T-gate" and "gamma-gate" processes are used in which the base or stem of the gate is very short (~100 nm) while the upper part is large, overlapping the stem, similar to a mushroom, or the letters T or Γ. Although such structures can be achieved using direct-write electron-beam lithography in double-layer resists, the technology is expensive, slow, and unlikely to meet future production needs. For these reasons,

we are developing a process for fabricating T-gates using x-ray lithography.

The fabrication sequence is shown in figure 25. The first layer defines the stem of the gate, a critical parameter for a field-effect device. After exposing and developing the first layer, a second layer of resist is deposited and the pattern corresponding to the upper part of the gate exposed. At this point, gate metal can be deposited forming the T-gate. Two challenges present themselves. First, it must be possible to align the x-ray masks to within 100 nm. Second, if the masks do not share a common coordinate system, features, such as the gate stem and mushroom, will not align properly. Also, without precision mask alignment, it would not be possible to get the gate stem very close to the source. Therefore, the three x-ray masks required in the process depicted in figure 25 must be written with reference to a coordinate system that is common to all of the masks. To meet the first challenge, we have put alignment marks on the masks that are compatible with the high precision, IBBI alignment system (see section 4.6). We anticipate no difficulty in achieving sub-100 nm alignment with the IBBI system.

To meet the second challenge, x-ray masks are prepared with a grid array of reference marks located at the corners of fields measuring 0.1 X 0.1 μm, the field size of the e-beam lithography system. These reference marks were transferred to each x-ray mask with DUV lithography using the same optical mask, thereby guaranteeing a common coordinate system for all three x-ray masks. Upon registration to these marks, the e-beam lithography system should be able to place patterns with a precision well below 100 nm.

There are a number of interesting directions that may be followed once a reliable, high-latitude process is established. For manufacturable MMIC systems, both MESFETs and HEMTs are required for low-noise and power applications. Initially, relatively simple GaAs MESFETs will be studied, followed by GaAs and InP HEMTs of varying degrees of complexity. Further studies could include low-temperature-grown GaAs MESFETs for high breakdown voltages, self-aligned devices, or gate materials other than Au, such as W.

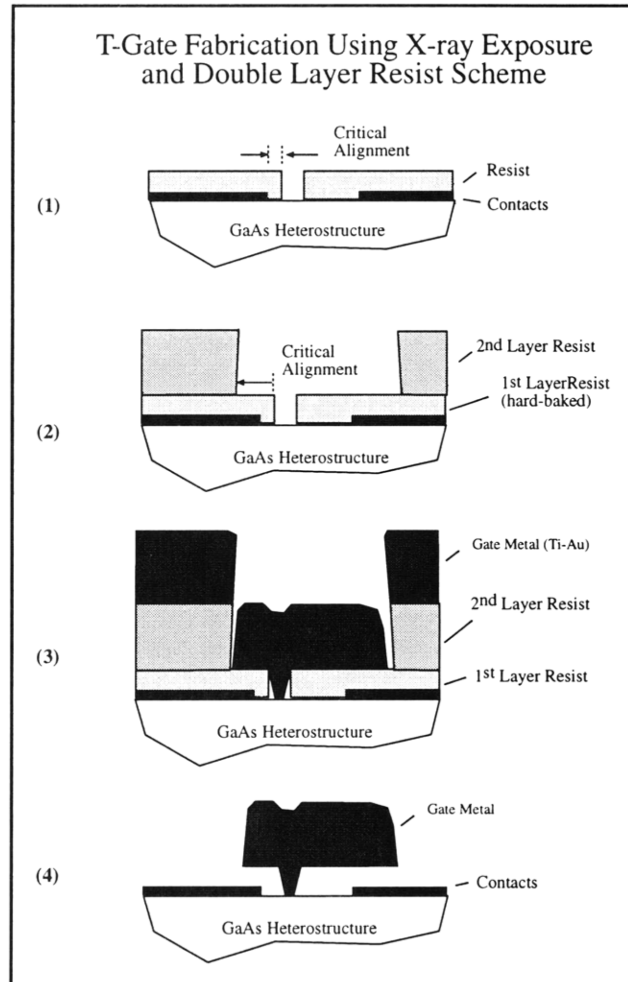

Figure 25. Depiction of the T-gate process steps: (1) resist is deposited over existing contact metal. Alignment and exposure takes place, (2) after hardening the first layer, a second layer is deposited. The second pattern alignment and exposure takes place, (3) gate metal is deposited, and (4) liftoff (resist removal).

4.11 Studies of Coulomb Charging Effects and Tunneling in Semiconductor Nanostructures

Sponsors

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Grant DAAH04-95-1-0038
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Project Staff

David J. Carter, Ilia Sokolinski, Professor Dimitri A. Antoniadis, Dr. Michael R. Melloch,[1] Professor Terry P. Orlando, Professor Henry I. Smith

Quantum-effect devices, whose minimum feature sizes are comparable to the Fermi wavelength (about 50 nm in a typical inversion layer), have promising potential in novel electronics applications. Quantum-dot devices have drawn particular attention. In such devices, an electron gas is confined electrostatically in all three dimensions, forming a small ~100 nm "island" of electrons bounded on all sides by potential walls. This small electron "island" resembles an atom in that there can be only an integer number of electrons, and these electrons can occupy only certain discrete energy levels. If two dots are coupled, a structure resembling a molecule is obtained. The conductance of the dot, when connected to leads through tunnel barriers, exhibits strong oscillations as the voltage of the gate is varied. Each successive conductance maximum corresponds to the addition of a single electron to the dot. At temperatures in the millikelvin range the conductance decreases by orders of magnitude in-between adjacent conductance maxima because there is a large energy cost for an electron in the lead to enter the dot. This energy cost can be removed by changing the gate voltage, resulting in the observed periodic dependence of the conductance on gate voltage. By opening up barriers between the dot and the outside world, the energy cost is also reduced and the Coulomb blockade breaks down.

Previous experiments in semiconductor structures have focused on quantum dots that are coupled to their environment or to each other via quantum-point-contacts (QPCs). As these QPCs are opened to allow the dot to couple to its electronic environment, a single-electron transport channel opens up. When one transport channel is opened fully (such that its transmission probability is equal to unity), the quantum dot no longer has a well-defined charge state and Coulomb blockade effects disappear.

We have fabricated a different type of quantum dot structure in which the transition from poor environmental coupling to strong coupling happens not through the opening of one channel to a transmission of unity, but through the opening of many channels to a small transmission probability. In this case, the physics of the transport will be much more like that of a metal tunnel barrier, such as those used in Josephson junctions or metal Coulomb blockade devices. Figure 26 shows the two types of double-dot structures, one with a QPC between the dots and one with a fine-line tunnel barrier between them. By fabricating both devices on the same chip, a number of experiments can be done comparing the behavior of the two barrier types in single and double-dot configurations.

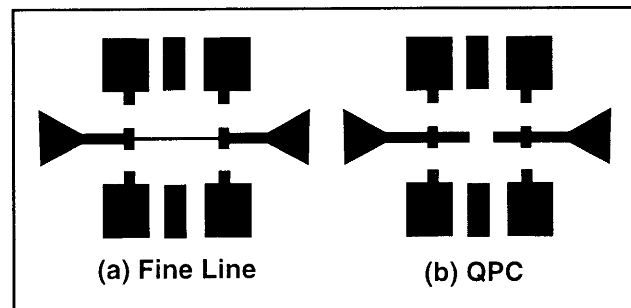

Figure 26. Schematic of two different types of coupled quantum dot devices. A two-dimensional electron gas (2DEG) is approximately 60 nm below the surface of a GaAs/AlGaAs heterostructure. Schottky gates on the surface, shown in black, electrostatically create lateral confinement. Regions where the 2DEG exists after biasing the Schottky gates are shown in light gray. When the barrier between the coupled dots is opened, the nature of the coupling between dots is quite different for the two structures.

In order to fabricate the tunnel barrier structure in such a way as to have good control over the strength of the barrier with an external voltage source, it is necessary to have extremely fine lines. In order to push these widths as low as possible, we used x-ray nanolithography, which has minimal line-widening effects due to backscattered electrons from the substrate as is found, for example, in an electron-beam direct-write process. A scanning-electron micrograph of the novel coupled-quantum-dot gate structure on a GaAs substrate is shown in figure 27.

[1] Purdue University, West Lafayette, Indiana.

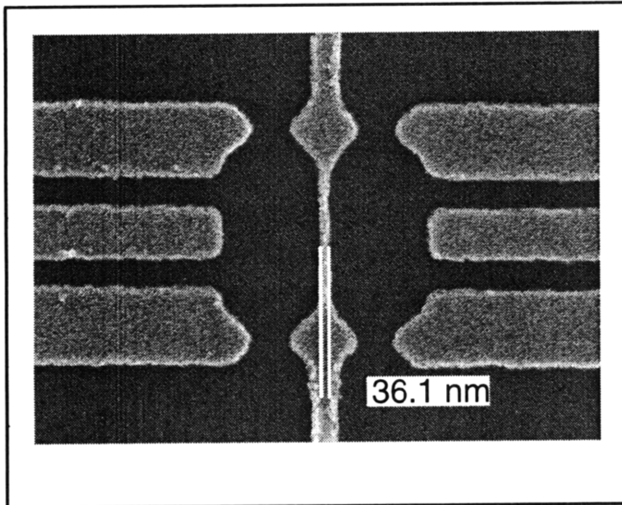

Figure 27. Scanning-electron micrograph of a coupled quantum dot device on a GaAs/AlGaAs heterostructure fabricated with x-ray lithography.

We have also fabricated a one-dimensional array of seven quantum dots. The device was fabricated by direct-write e-beam lithography on a non-back-gated GaAs/AlGaAs heterostructure. Figure 28 shows the scanning-electron micrograph of a completed test device. The size of the dots in the measured device was 500 X 600 nm^2.

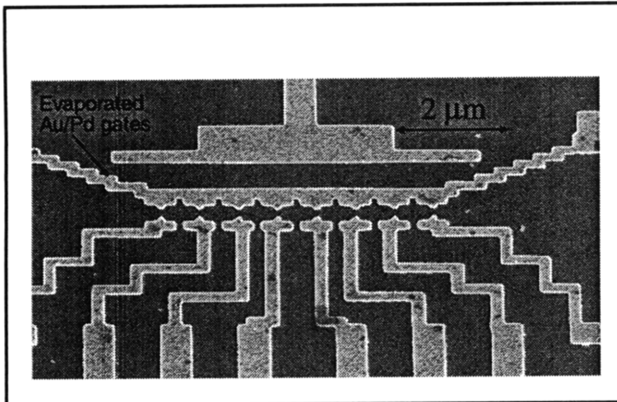

Figure 28. Scanning-electron micrograph of a quantum dot array device on a GaAs/AlGaAs heterostructure fabricated with e-beam lithography.

We have conducted initial low-temperature measurements of our device, and reproduced a double dot experiment, first reported by Waugh et al. A schematic of the experiment is shown in figure 29a.

A double quantum dot was created by applying appropriate voltages to gates M, G5, G6 and G7. The side-gate was then swept and Coulomb blockade oscillations were observed. Figure 29b shows changes in the pattern of Coulomb blockade oscillations with increasing inter-dot coupling. The voltage on G6 was increased by 20 mV for each subsequent curve increasing conductance through QPC6 and thus increasing inter-dot coupling. We see that for a bottom curve, the period oscillations is 24 mV (corresponding to C_{sg} = 7aF). Thus, for a system of two identical quantum dots we observe a regular peak period equal to the peak period a single dot. On the next several curves, each peak is split into two peaks which move farther apart as the inter-dot coupling increases. Finally, on the top curve, we again see regular Coulomb blockade peaks, but with a different period Q 9 mV (corresponding to C_{sg} = 18aF). For this curve, the two original dots merged into one large dot which has approximately twice the capacitance to the gate.

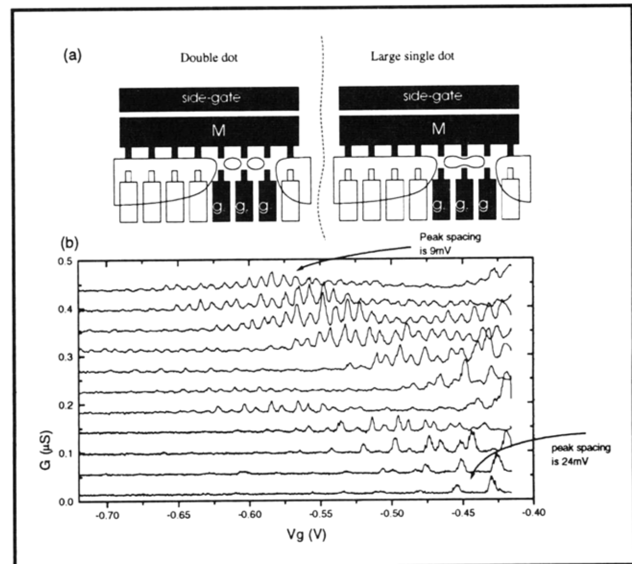

Figure 29. (a) Schematics of double dot experiment. By applying appropriate voltages to gates M, G5, G6 and G7, one can create either a double dot or a single large dot depending of the voltage on G6. (b) Experimental results. On the bottom curve QPC G6 is closed, so we have a double dot. As the conductance of quantum-point-contact (QPC) G6 is increased for each subsequent curve each peak is split into two. When QPC G6 is open enough so that we have a single dot, the peak spacing becomes approximately half of the period for the double dot.

4.12 Fabrication and Transport Studies of Lateral Surface Superlattices in GaAs/AlGaAs Modulation Doped Field-Effect Transistors

Sponsor

U.S. Air Force - Office of Scientific Research
Grant F49620-95-1-0311

Project Staff

Anne Pepin, Mark R. Schweizer, Professor Dimitri A. Antoniadis, Dr. Michael R. Melloch,[2] Professor Terry P. Orlando

We are investigating lateral-surface superlattice (LSSL) devices. Figure 30 shows this device is similar to conventional high-electron-mobility transistors, but the gate is a metallic grid of fine period (150 - 400 nm), rather than the conventional continuous gate. Electrons under this gate see a periodic potential which is tunable by controlling the gate bias. The imposed periodic potential creates minibands superimposed on the band structure created by the crystalline periodic potential. In earlier research, we observed electron back diffraction in 200 nm period, 65 nm-linewidth grid-gate structures. Additionally, negative differential conductance (NDC) was measured in devices with high source-to-drain bias applied. The NDC effect was attributed to sequential-resonant tunneling.

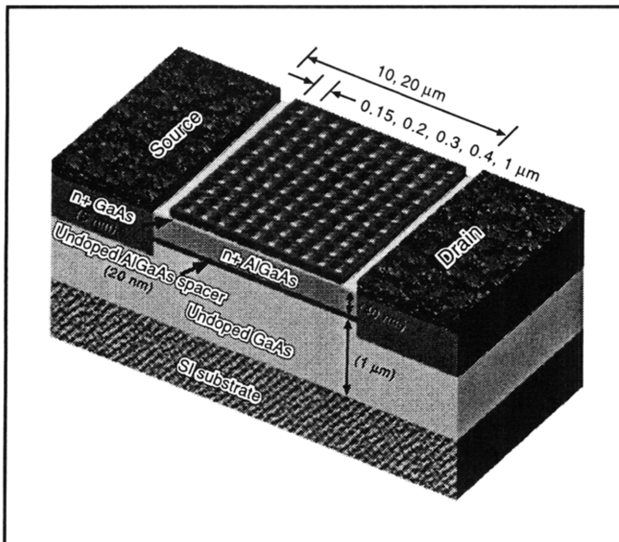

Figure 30. Schematic of the lateral surface superlattice device.

Our current focus is to better understand the high source-to-drain bias operation of the device and the phenomena of negative differential conductance. Our latest design allows for devices with a variety of periods (150, 200, 300, 400 nm, and 1 μm) as well as two separate gate lengths (10 and 20 μm) for each period.

4.13 Single-Electron Transistor Research

Sponsor

Joint Services Electronics Program
Grant DAAH04-95-1-0038

Project Staff

David B. Berman, Professor Raymond C. Ashoori, Professor Henry I. Smith

The single-electron transistor (SET) has the highest charge sensitivity of any man-made device. In many respects, it is the electric analog of the superconducting quantum interference device (SQUID), which is the most sensitive detector of magnetic field. It is very well suited for applications where one needs to measure small fluctuations of charge without disturbing the system under study. An example of such a system is a quantum dot.

Figure 31 shows a scanning-electron micrograph of one of our devices. The SET consists of an aluminum metal island connected to the source and drain electrodes by two thin, Al_2O_3 tunnel junctions. Fabrication of the tunnel junctions is done using the shadow evaporation method developed by Fulton and Dolan.

The operation of the SET depends on the fact that the central island has a very small capacitance and the energy that it takes for electrons to charge this island is quite large. For example, if the device is cooled to temperatures below 1 K, the electron thermal (kT) energy becomes less than the charging energy ($e^2/2C$). This means that without a significant source-drain voltage bias, the electrons cannot travel through the central island. This effect is known as the Coulomb blockade. The Coulomb blockade is manifested as a zero current region in the current-voltage dependence of the SET. This effect is shown in figure 32. The addition of gate voltage can alter the size of the Coulomb blockade region, thus we can use this device as a transistor.

[2] Purdue University, West Lafayette, Indiana.

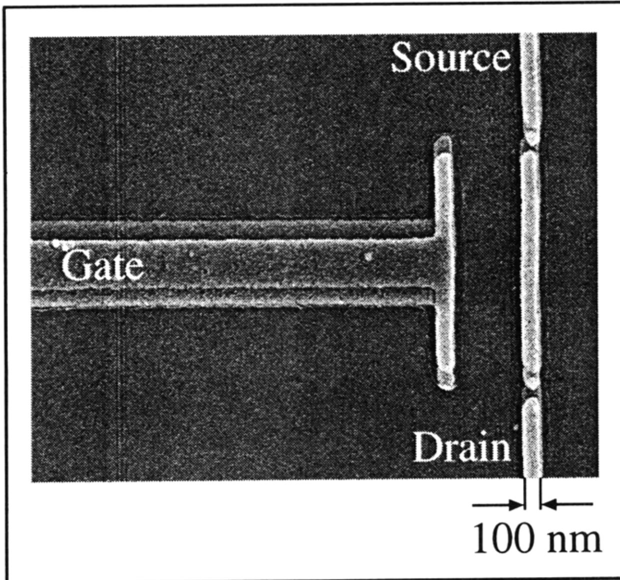

Figure 31. Scanning-electron micrograph of a single-electron transistor, made of Al, in which the two tunnel barriers are produced by a two-angle evaporation process.

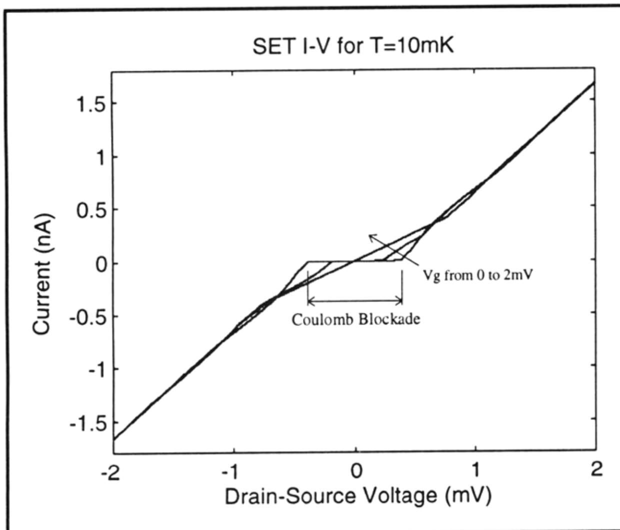

Figure 32. Current-voltage characteristic of a single-electron transistor taken at 10 mK, for three values of gate voltage. The Coulomb blockade is maximum at zero gate bias.

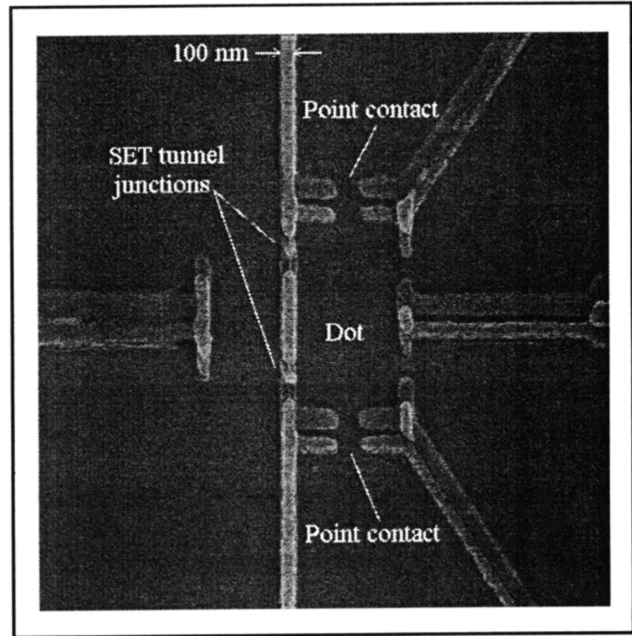

Figure 33. Scanning-electron micrograph of a lateral quantum dot experiment. The quantum dot is defined electrostatically in the two-dimensional electron gas below the surface by applying negative voltage to the metal leads on top. The single-electron transistor is fabricated in the lead pattern, such that the central island is located next to the quantum dot for good electrostatic coupling.

We have incorporated our technique of fabricating SETs into experiments with quantum dots. Figure 33 shows a micrograph of the device we are studying. The quantum dot is created in the 2DEG below the surface by applying a negative voltage to the metal leads on the surface and depleting the electrons below. The SET is integrated into the lead pattern defining the quantum dot and is used to detect any electrostatic changes in the dot.

In one of the experiments on this sample, we tested the effect of point-contact resistance on the Coulomb blockade in the quantum dot. Figure 34 shows a sample of the data from this experiment. One of the point contacts to the quantum dot is completely pinched off so there is no conduction through it. The other point contact is slowly closed as voltage on one of the gates is scanned. The onset of Coulomb blockade occurs when the point contact resistance is approximately 50 kohms.

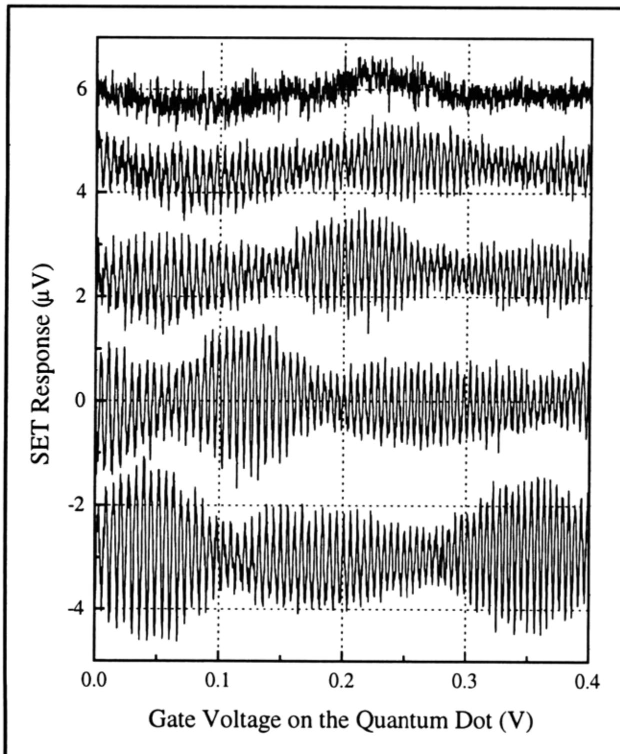

Figure 34. The signal from the single-electron transistor as the gate of the quantum dot is varied. One of the point contacts is completely pinched off, and the resistance of the other is slowly increased from the top trace to the bottom one. The point contact resistance is increased from about 10 kohms (top trace) to 100 kohms (bottom trace). The quantization of charge, or the appearance of single-electron peaks in the signal, appears for a point contact resistance of about 50 kohms.

4.14 One-Dimensional Photonic Band Gap Devices in SOI Waveguides

Sponsors

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Contract DMR 94-0034

Project Staff

Juan Ferrera, James S. Foresi, Pierre R. Villeneuve, Professor John D. Joannopoulos, Professor Lionel C. Kimerling, Professor Henry I. Smith

Photonic band gap (PBG) devices are optical analogs of semiconductors. A lightwave traveling through a PBG structure encounters a large, periodic change in the dielectric constant. The periodicity causes bands of frequencies to be disallowed from propagating through the device. These PBG devices are similar to distributed Bragg reflectors (DBRs), but have band gaps as large as 20 percent of the mid-gap frequency. The band gaps for DBRs are typically less than 1 percent. PBG's can be designed in one, two, and three dimensions. In this project we are developing 1-D PBGs that are directly integrated into silicon waveguides. Their band gap is centered at $\lambda = 1.54\ \mu m$. This wavelength is compatible with fiber optic communication systems.

The 1-D PBG device consists of a single-mode strip waveguide fabricated from SOI material with a periodic series of holes etched through the Si. The large dielectric contrast between the Si and the holes (12:1) results in a band gap of 15 percent of the mid-gap frequency. The waveguide width is approximately 0.55 μm, with holes of 0.3 μm diameter, spaced at 0.48 μm. The minimum dimensions, 0.1 μm, occur between the holes, and between the edges of the waveguide and the edge of the holes. Because of the small feature size we use a combination of e-beam and x-ray lithography for patterning. To minimize possible alignment errors, we fabricated an x-ray mask that contained both the waveguide structure and the hole structures together. E-beam writing these long (typically 2 μm) waveguide devices required stringent control of e-beam field stitching.

To fabricate the devices, we begin with an SOI substrate, a 0.2 μm silicon layer on a 1.0 μm oxide layer. The relatively thick oxide is required to keep the optical mode of the waveguide from leaking into the substrate. The wafer is then coated with PMMA and the pattern transferred to the PMMA via x-ray lithography. The PMMA is developed and a 50 nm Cr layer evaporated onto the sample. The PMMA is then dissolved in acetone and the Cr that is in direct contact with the Si remains as the etch mask. The Si layer is etched in a CF4 plasma with 15 percent O_2. An additional etch into the oxide is performed using CHF_3. The oxide etch has been shown theoretically to improve the performance of the PBG device.

An SEM image of a completed PBG waveguide device is shown in figure 35. This device, which consists of two sections of four holes each separated by a gap, is a microcavity. Light is localized in the region between the two sets of holes. The two sets of holes act as two mirrors forming a resonant cavity within the waveguide. This type of resonant structure is expected to have a high quality factor (Q~500) with applications ranging from the control of spontaneous emission of light emitting materials to channel dropping filters for wavelength division multiplexing. The transmission through this device has been calculated and is shown in figure 36. Transmission near 90 percent is expected at the resonant wavelength of 1.55 μm.

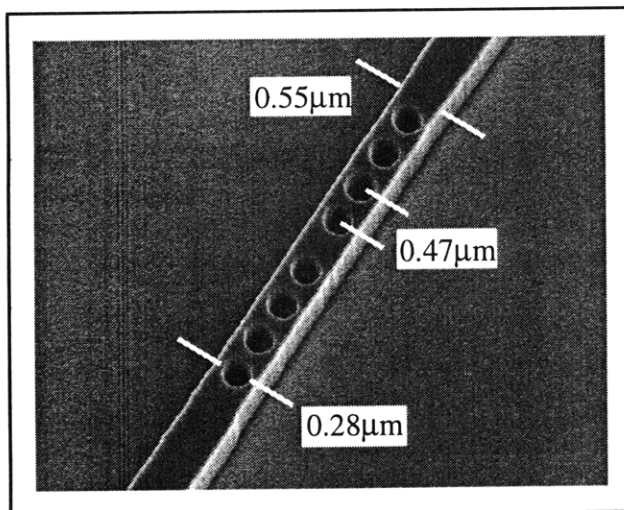

Figure 35. Scanning-electron micrograph of 1D photonic-bandgap microcavity in Si on SiO_2, fabricated using e-beam and x-ray lithographies, Cr liftoff, and reactive ion etching.

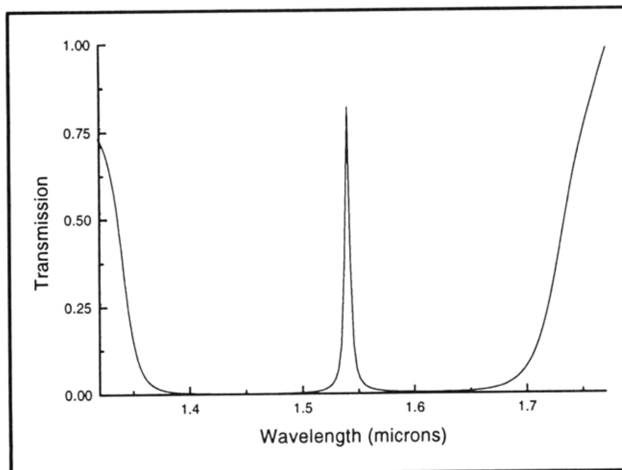

Figure 36. Calculation of optical transmission through the 1D photonic bandgap microcavity.

4.15 Fabrication of Grating-Based Optical Filters

Sponsors

National Science Foundation
Grant ECS 94-07078
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Contract F49620-96-0126

Project Staff

Dr. Jay N. Damask, Juan Ferrera, Michael H. Lim, Thomas E. Murphy, Professor Hermann A. Haus, Professor Leslie A. Kolodziejski, Professor Henry I. Smith

Grating-based optical filters require Bragg-grating corrugations to be patterned on top of a waveguide structure. Ideally, the grating patterns self-align to the waveguide pattern so as to isolate the gratings to the top of the waveguide, the k-vector of the grating runs parallel with the local direction of the waveguide, and all lithographies are done on a planar surface prior to etching either the grating or waveguide. We have conceived a new fabrication technique that elegantly satisfies all the above criteria.

Traditional thinking on how to pattern the waveguides and gratings required that the waveguides are patterned and etched first; then the gratings were aligned to the waveguides, patterned, and etched. This process required one particularly difficult step where the mask that resisted the waveguide etch had to be "reversed" after the etch. Reversal means that the areas that just etched had to be covered with a second mask while the tops of the waveguides in particular regions had to be exposed for the subsequent grating patterning. This process was successful after some difficulties; summaries of the results appear in the MIT 1994 and 1995 *RLE Progress Reports*. However, if there is an error in the mask reversal phase of the process, nothing can be done to correct it, and the yield is nothing. Moreover, as the waveguide heights increased, and the tolerance to k-vector misalignment between the grating and the waveguide was decreased, the above process became less attractive.

The new process avoids these problems in a somewhat counter-intuitive way. First, the gratings are patterned before the waveguides, but the waveguides will be etched before the gratings are etched. Second, in order to pattern the gratings on the top surface, it is pre-patterned with photoresist in the grating regions only. The advantage of the combination of these two steps is that the gratings are self-aligned to the waveguide shapes and that, if there is an error in the grating print, or the subsequent waveguide print, all the hard masks can be stripped, and the fabrication process started anew without destroying the sample.

Figures 37 to 40 illustrate the sequence of processing steps for the two lithographies and hard masks. The material for the first and second hard masks must be chosen so that either mask can be etched away without etching either the remaining hard mask or the exposed surface of the waveguide core. The use of silicon and chromium is one example of a compatible pair of hard masks for a glass waveguide system.

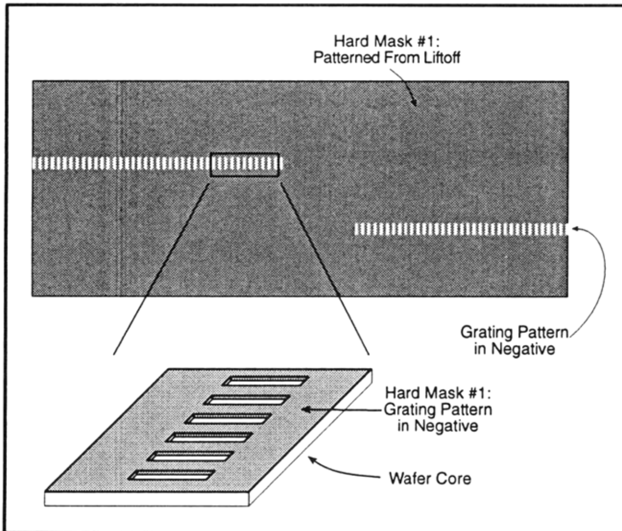

Figure 37. First, PMMA is spun on a planar waveguide core layer. Second, the wafer is exposed with an optical mask to delineate "grating windows." All the resist is developed away except in regions where the gratings will be printed. Third, the PMMA is exposed to an x-ray or phase mask that holds the grating. Finally, after resist development, a metal mask is lifted off, resulting in an entirely masked substrate except where the grating patterns reside.

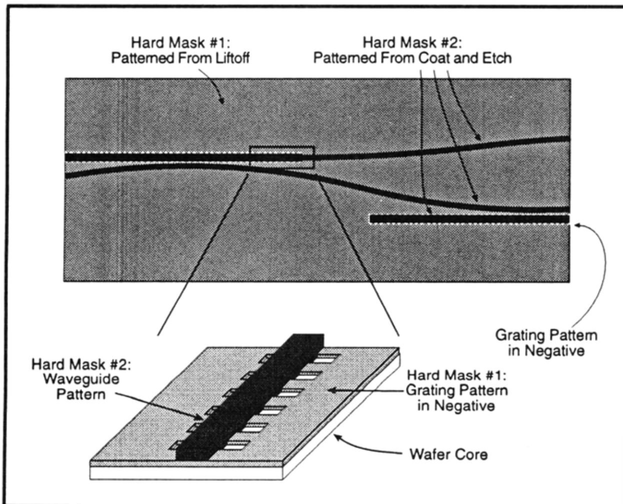

Figure 38. Following the preceding step, the entire surface is coated with a second hard mask. The grating mask from the preceding step held alignment mark targets which are directly aligned with e-beam lithography to the k-vector of the gratings. A second optical mask, the waveguide mask, holds complimentary alignment marks which align to the grating target marks. Once the waveguide mask is aligned to the wafer, the resist is developed and used as a mask to etch away the second hard mask. The result is a second hard mask which holds the shape of the waveguides, patterned over the grating teeth.

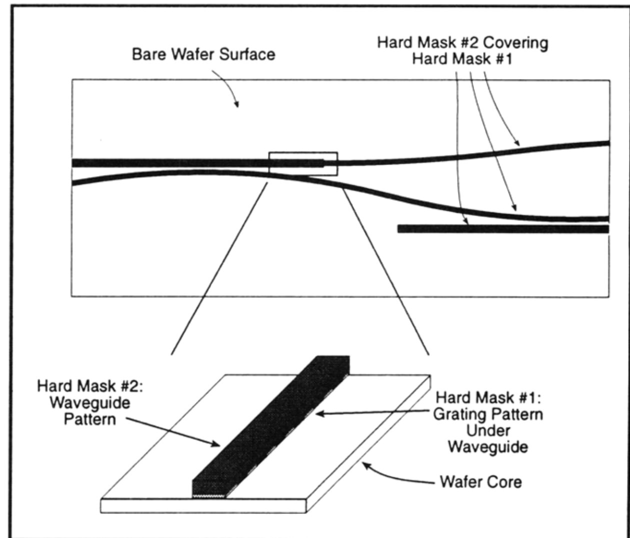

Figure 39. The second hard mask is used as a mask to etch away the first hard mask, originally lifted off after the grating point. The result is a self-aligned grating pattern which resides under the waveguide pattern.

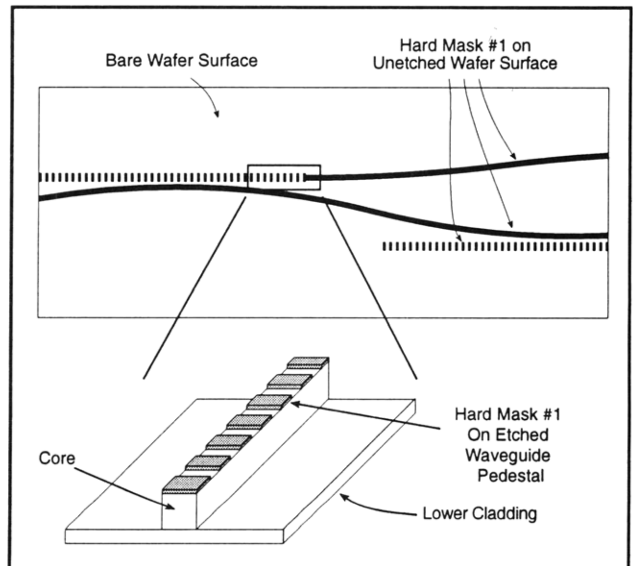

Figure 40. The waveguide rib or channel is etched using the second hard mask. Then, the second hard mask is stripped, revealing the first hard mask, which contains the grating pattern. The waveguide is then etched a second time to transfer the grating to the waveguide. The first hard mask is then stripped, revealing the complete formation of the waveguide and grating. An upper cladding layer may then be deposited to complete the waveguide.

What is not illustrated in the figures is how the k-vector of the grating is aligned to the waveguide. Prior to the alignment of the grating x-ray mask to the pre-patterned substrate, alignment marks are written with e-beam lithography onto the grating mask. The alignment marks on the grating mask not only compliment the target marks on the substrate pre-pattern, but they are written so as to align

precisely to the grating lines themselves. Specifically, one mark on the grating mask is written. Then, one grating line is identified and followed along the length of the mask to the second alignment mark location. The second mark is written in alignment with the grating as well as in the general location of the target on the substrate pre- pattern. This process is repeated until all requisite alignment marks are written. These marks are then aligned to the wafer pre-pattern.

To date, two device mask systems, the optical matched filter and the resonant channel-dropping filter, are being fabricated in the manner presented above. The material systems are the germium-doped silicon dioxide and the InGaAsP/InP compound semiconductor.

4.16 Integrated Optical Grating-Based Matched Filters for Fiber-Optic Communications

Sponsors

National Science Foundation
Grant ECS 94-07078
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Contract F49620-96-0126

Project Staff

Thomas E. Murphy, Dr. Jay N. Damask, Juan Ferrera, Michael H. Lim, Professor Hermann A. Haus, Professor Henry I. Smith

The unavoidable presence of noise in optical communications systems makes it necessary to use filters to obtain the best performance. The most sensitive optical receivers demonstrated to date utilize optical preamplification before detection. While the optical preamplifier can provide substantial gain, it is also the dominant source of noise in the system. The sensitivity of the optical receiver is depends upon how well the optical data signal can be separated from this background noise.

The noise from an optical amplifier is broad-band in nature, and usually overlaps the narrow-band communications channel. For this reason, the most suitable filter is one which has a spectral response similar to the signal to be detected. This project seeks to develop an optical matched filter; a filter whose spectral response is precisely matched to the communications signal of interest. Such a filter can be shown to yield the highest signal-to-noise ratio and therefore, the best performance.

Figure 41 depicts a typical 10 Gb/s optical data signal, consisting of a sequence of square pulses 100 ps in duration each representing a single bit. The corresponding signal spectrum has the characteristic sinc shape, centered at the optical carrier wavelength of 1.55 μm.

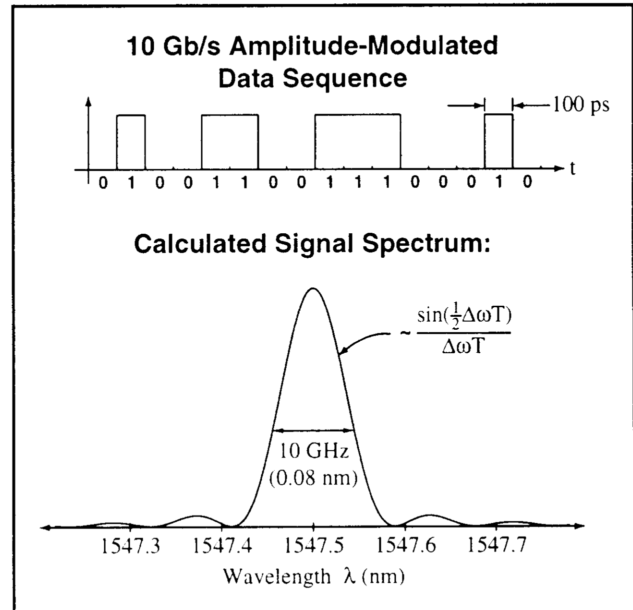

Figure 41. A typical 10 Gb/s binary encoded optical signal, and the corresponding predicted signal spectrum. Note that only the slow 10 GHz amplitude modulation is depicted in the pulse diagram. The rapid oscillations associated with optical carrier frequency are not shown.

To date, it has been difficult to achieve an optical filter response that is precisely matched to the spectrum depicted in figure 41; communications engineers must instead settle for one that resembles, but does not match the spectrum.

However, the reflection spectral response of a properly designed weak Bragg grating can match the spectrum of the incident pulse stream, thereby providing a convenient way to realize a matched filter.

Figure 42 depicts a weak Bragg grating filter, constructed in a Mach-Zehnder interferometer. The grating is formed by etching a shallow periodic pattern onto the top surface of the waveguide structure. The Mach-Zehnder configuration provides a means of spatially separating the reflected signal from the input signal. In this device, two identical grating filters are placed in opposite arms of a Mach-Zehnder interferometer. Light is launched in the upper port of the device and a codirectional coupling region transfers half of the signal to the lower waveguide. A portion of the light in each arm of the interferometer is reflected by the two identical weak gratings. The reflected signals recombine in

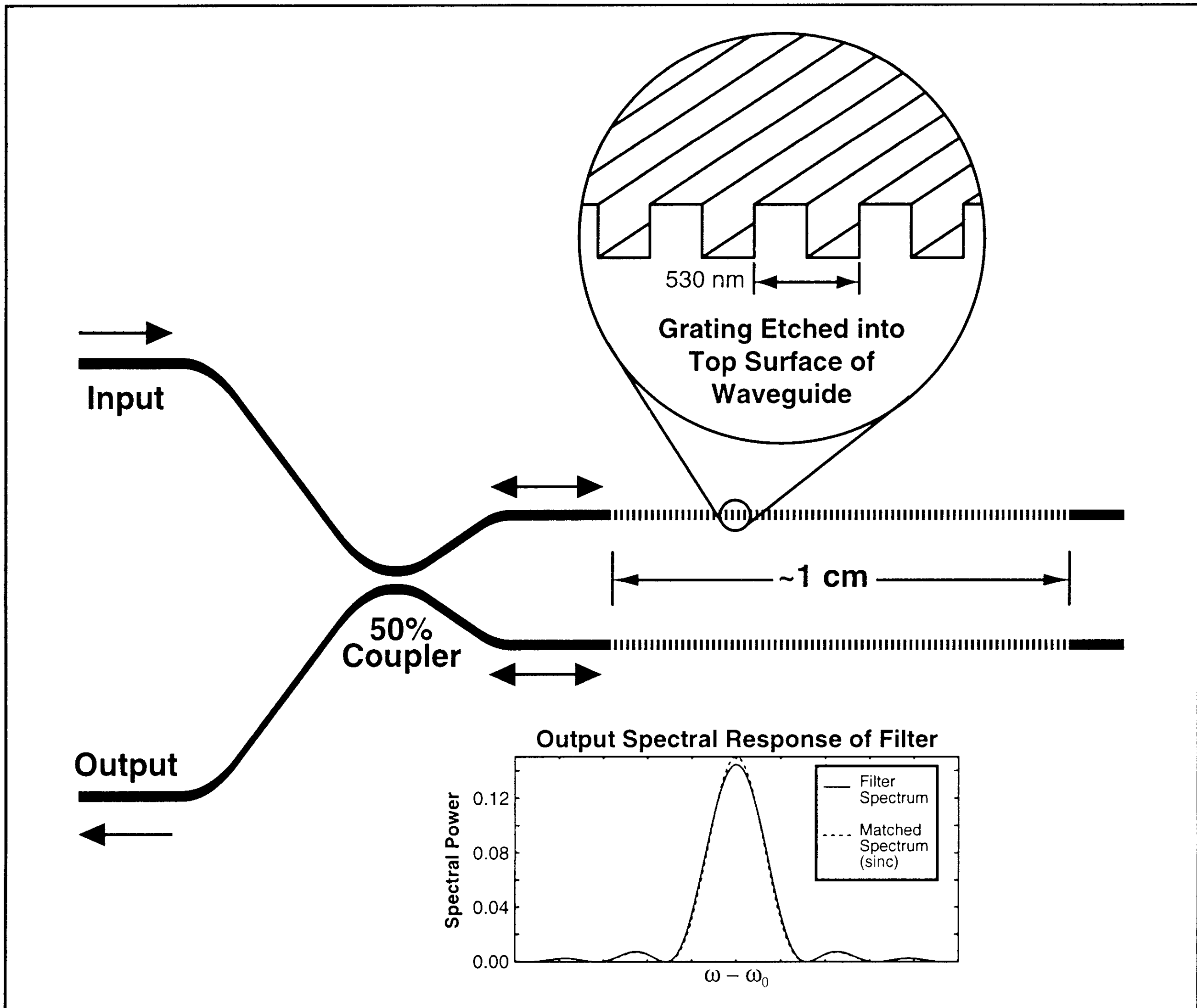

Figure 42. A schematic diagram of an integrated matched filter. Two identical weak Bragg gratings are constructed in a Mach-Zehnder configuration, which provides spatial separation of the input signal and the filtered signal.

the 50 percent coupling region and emerge in the lower port of the device.

Because the device is constructed on an optical chip, it offers the potential for integration with other optical and electronic components of the receiver system. Moreover, the planar fabrication approach makes it possible to use precision alignment techniques to control the dimensions of the device to within a fraction of a wavelength of light.

Presently, our work on this project is concentrated on developing the fabrication technologies for building this device. The grating portion of the device consists of fine-period patterns (~250 nm lines and spaces) that must be spatially coherent over distances as large as 1 cm. We use interferometric lithography to generate these grating patterns on an x-ray mask. The grating patterns can then be transferred to the waveguides using x-ray lithography and reactive-ion etching. Optical lithography is used to print the larger waveguide features on the substrate.

One of the important fabrication challenges that we are currently addressing is the need to have the gratings aligned in angle to the waveguide patterns on the device. Misalignment of the gratings to the waveguides will lead to undesirable back-reflection in the input port of the device. In order to address this problem, we plan to use electron-beam lithography to add alignment marks to the x-ray mask. Using an electron-beam system, the alignment marks can be placed such that they are perfectly aligned in angle with the interferometrically generated grating lines.

With this device, we hope to push towards the theoretical limit of receiver sensitivity: preamplified optical receivers which can reliably detect signals as weak as 40 photons per bit. Additionally, we believe that developing the fabrication technology for these devices will enable us to consider a variety of related integrated-grating devices for other optical communications applications.

4.17 High-Dispersion, High-Efficiency Transmission Gratings for Astrophysical X-ray Spectroscopy

Sponsor

National Aeronautics and Space Administration
Contract NAS8-38249

Project Staff

Robert C. Fleming, Jeanne M. Porter, Jane D. Prentiss, Robert D. Sisson, Dr. Joost van Beek, Professor Claude R. Canizares, Dr. Mark L. Schattenburg, Professor Henry I. Smith

Through a collaboration between the Center for Space Research (CSR), the NanoStructures Laboratory (NSL), and the Microsystems Technology Laboratory (MTL), x-ray transmission gratings are fabricated for the NASA Advanced X-ray Astrophysics Facility (AXAF) x-ray telescope, scheduled for launch on the Space Shuttle in 1998. This major national facility will provide high-resolution imaging and spectroscopy of x-ray-emitting astrophysical objects, with unprecedented power and clarity, promising to significantly widen our view of the universe.

Many hundreds of large area, gold transmission gratings with 200 nm and 400 nm periods are required for the high-energy transmission grating spectrometer (HETGS) on AXAF, which will provide high-resolution x-ray spectroscopy in the 100 eV to 10 keV band. In order to achieve spectrometer performance goals, the gratings need to have very low distortion (< 200 ppm), and high-aspect-ratio structures, significantly pushing the state-of-the-art of nanofabrication.

The need for high grating quality, and an aggressive production schedule, demanded the development of a robust, high-yield manufacturing process. We adopted a scheme involving interferometric lithography with tri-level resist, followed by cryogenic reactive-ion etching and gold electroplating (see figure 43). A chemical etching step then yields membrane-supported gratings suitable for space use. The gratings undergo extensive testing before being assembled in the spectrometer.

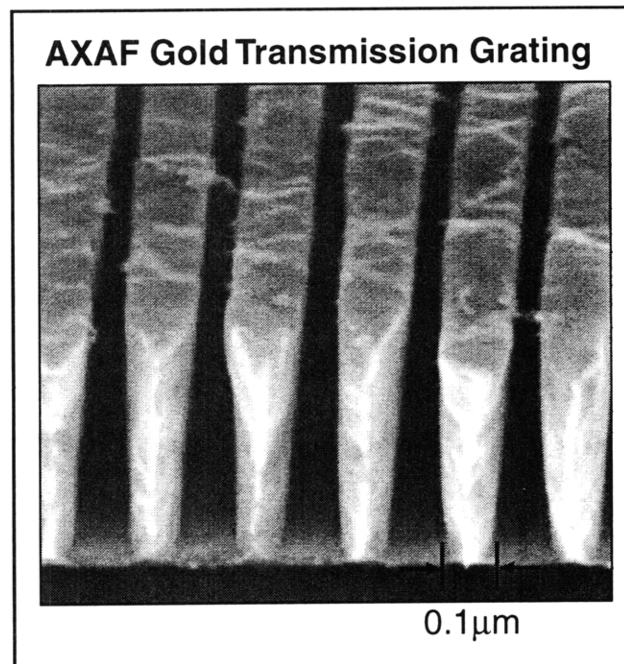

Figure 43. Scanning-electron micrograph of a 200 nm-period gold x-ray transmission grating, cleaved to show the 500 nm-thick line sidewalls.

A new cleanroom fabrication facility was built (the Space Microstructures Laboratory, on the 4th floor of Building 37 adjacent to the Gordon Stanley Brown Building), in order to fabricate the AXAF gratings. The proximity of the new lab to the MTL allows the sharing of many services such as DI and process water, nitrogen, process vacuum, and waste drains. The SML space includes 1700 square-feet of Class 100 and associated support areas, and a large complement of state-of-the-art equipment. Production of flight gratings has now been completed and flight spares production is underway. In October 1996, NASA took delivery of the completed HETGS flight instrument (figure 44), which is now undergoing calibration and integration.

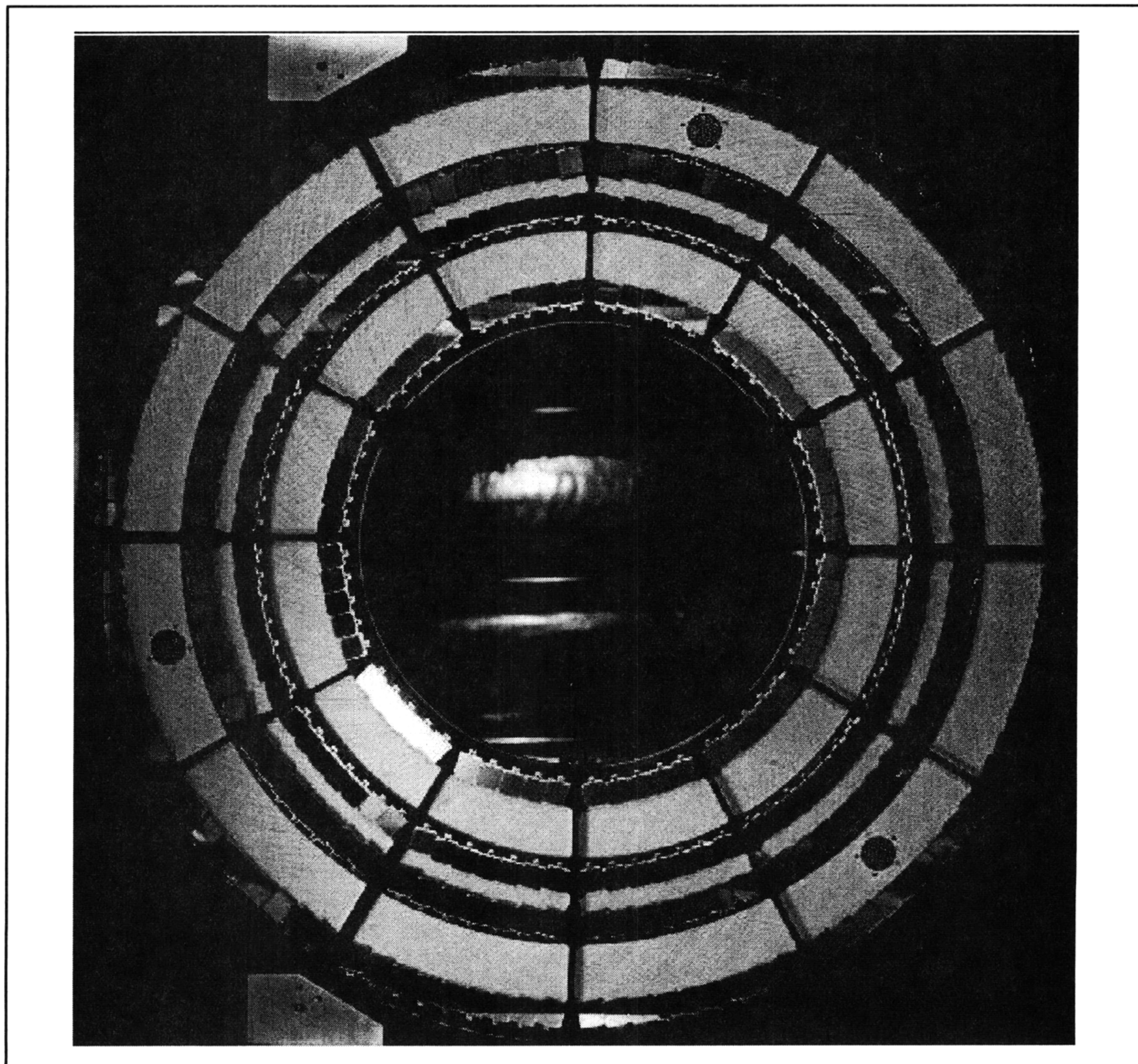

Figure 44. Photograph of the HETGS flight instrument, which consists a 1.0 meter-diameter aluminum wheel populated with hundreds of 200 nm and 400 nm-period gold x-ray transmission gratings (340 total).

4.18 Submicrometer-Period Transmission Gratings for X-ray and Atom-Beam Spectroscopy and Interferometry

Sponsors

Joint Services Electronics Program
Grant DAAH04-95-1-0038
National Aeronautics and Space Administration
Contract NAS8-38249
Grant NAGW-2003

Project Staff

James M. Carter, Jeanne M. Porter, Timothy A. Savas, Dr. Mark L. Schattenburg, Professor Henry I. Smith

Transmission gratings with periods of 100-1000 nm are finding increasing utility in applications such as x-ray, vacuum-ultraviolet, and atom-beam spectroscopy and interferometry. Over 20 laboratories around the world depend on MIT-supplied gratings in their work. For x-ray and VUV spectroscopy, gratings are made of gold and have periods of 100-1000 nm, and thicknesses ranging from 100-1000 nm. They are most commonly used for

spectroscopy of the x-ray emission from high-temperature plasmas. Transmission gratings are supported on thin (1 μm) polyimide membranes or made self supporting ("free standing") by the addition of crossing struts (mesh). (For short x-ray wavelengths, membrane support is desired, while for the long wavelengths a mesh support is preferred in order to increase efficiency.) Fabrication is performed by interferometric lithography combined with reactive-ion etching and electroplating. Progress in this area tends to focus on improving the yield and flexibility of the fabrication procedures.

Another application is the diffraction of neutral atom and molecular beams by mesh supported gratings. Lithographic and etching procedures have been developed for fabricating free-standing gratings in thin silicon nitride (SiN_x) supported in a Si frame. Figure 45 shows a free-standing 100 nm period grating in 1000 Å-thick silicon nitride.

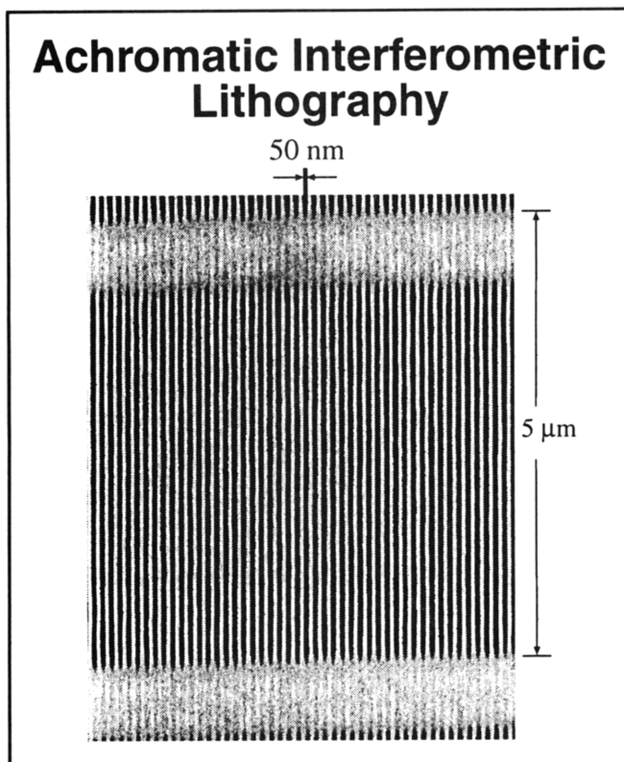

Figure 45. Scanning electron micrograph of a free-standing 100 nm period grating in a silicon nitride membrane of area 500 μm by 5 μm.

We have established a collaboration with the Max-Planck Institute in Göttingen, Germany, in which they utilize our gratings of 100 nm period in diffraction experiments using He atom beams. Figure 46 shows a spectrum obtained by diffracting a He beam through a 100 nm-period transmission grating. In addition, we have established a collaboration with Professor David E. Pritchard at MIT. His group will use our 100 nm-period gratings in diffraction and interferometer experiments using neutral sodium atom beams.

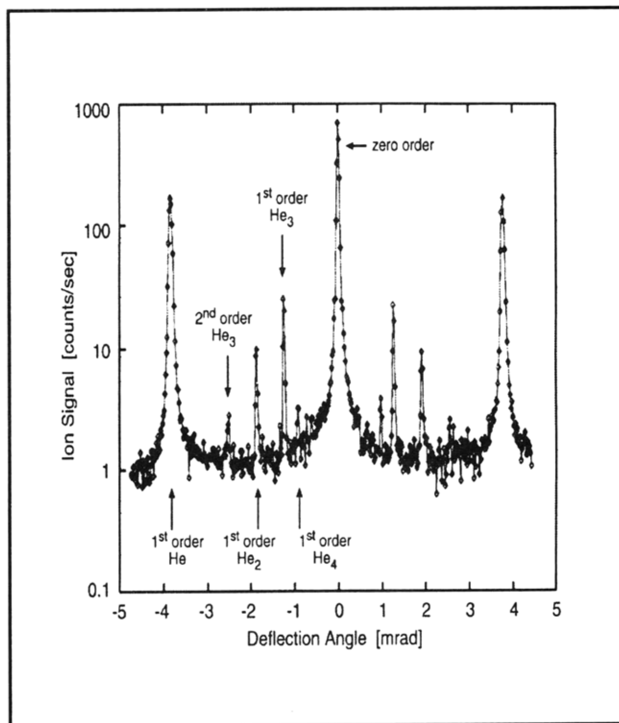

Figure 46. Helium beam diffraction spectrum. These results were obtained by Wieland Schollkopf and Peter Toennies at the Max-Planck Institute in Göttingten, Germany.

4.19 Super-smooth X-ray Reflection Gratings

Sponsors

Harvard-Smithsonian Astrophysical Observatory
Contract SV630304
National Aeronautics and Space Administration
Grant NAG5-5105

Project Staff

Dr. Joost van Beek, Robert C. Fleming, Andrea E. Franke, Jeanne M. Porter, Jane D. Prentiss, Robert D. Sisson, Dr. Mark L. Schattenburg, Professor Claude R. Canizares, Professor Henry I. Smith

Grazing-incidence x-ray reflection gratings are an important component of modern high-resolution spectrometers and related x-ray optics. These have traditionally been fabricated by diamond scribing with a ruling engine, or more recently, by interferometric lithography followed by ion etching. These methods result in gratings which suffer from

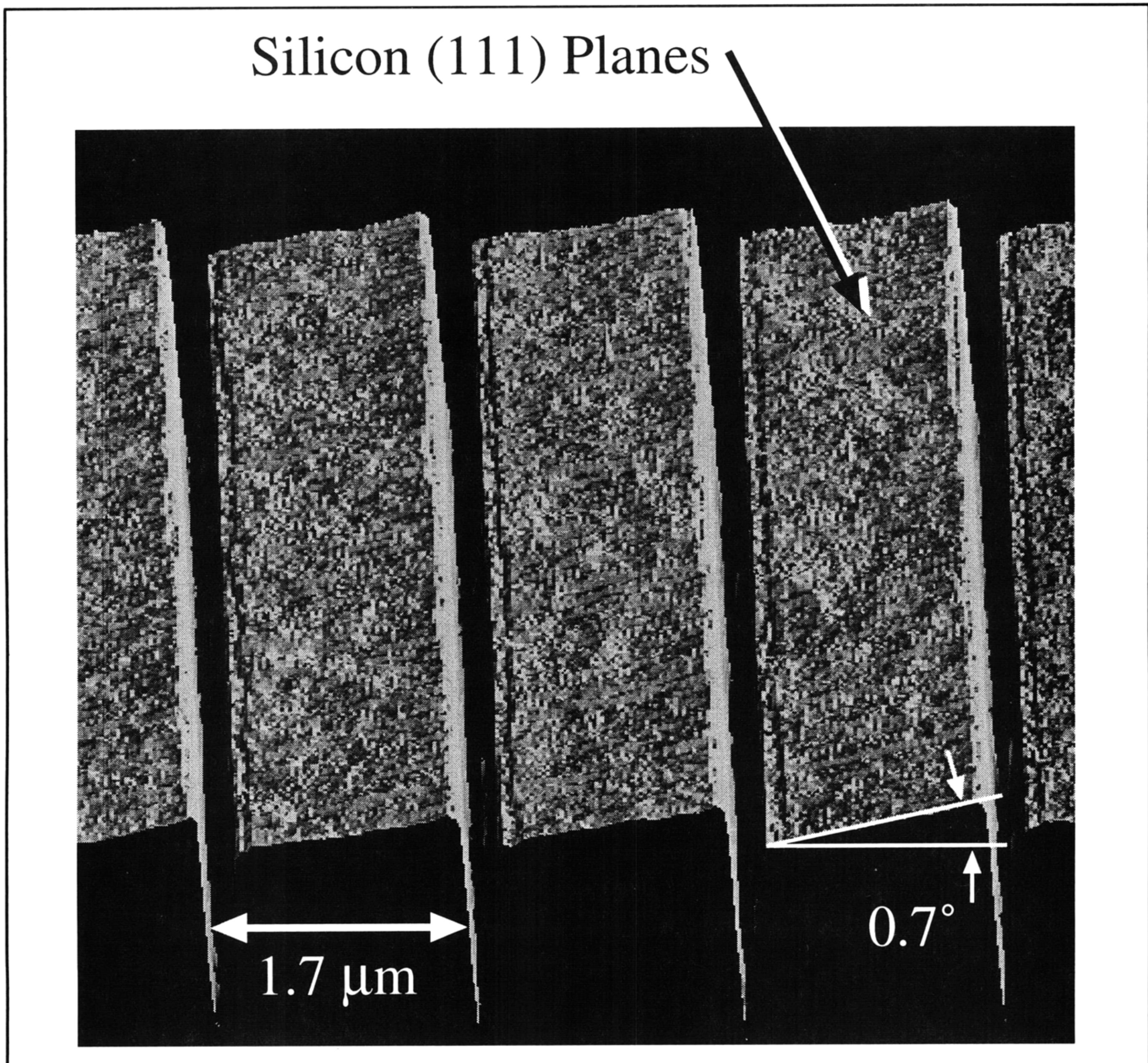

Figure 47. An AFM image of a traditional mechanically-ruled and replicated x-ray reflection grating. Note the rough, wavy grating surfaces which lead to poor diffractive performance.

a number of deficiencies, including high surface roughness and poor groove profile control, leading to poor diffraction efficiency and large amounts of scattered light (see figure 47).[3]

We are developing improved methods for fabricating blazed x-ray reflection gratings which utilize special (111) silicon wafers which are cut 0.7 degrees off from the (111) plane. Silicon anisotropic etching solutions such as potassium hydroxide (KOH) etch (111) planes extremely slowly compared to other crystallographic planes, resulting in the desired super-smooth blaze surface. Previous work used similar off-cut (111) silicon substrates to fabricate blazed diffraction gratings. However, that method utilized a second KOH etch step which compromised the grating facet flatness and is unsuitable for small grazing angle x-ray diffraction.

3 Bixler et al., *Proc. SPIE* 1549: 420-428 (1991).

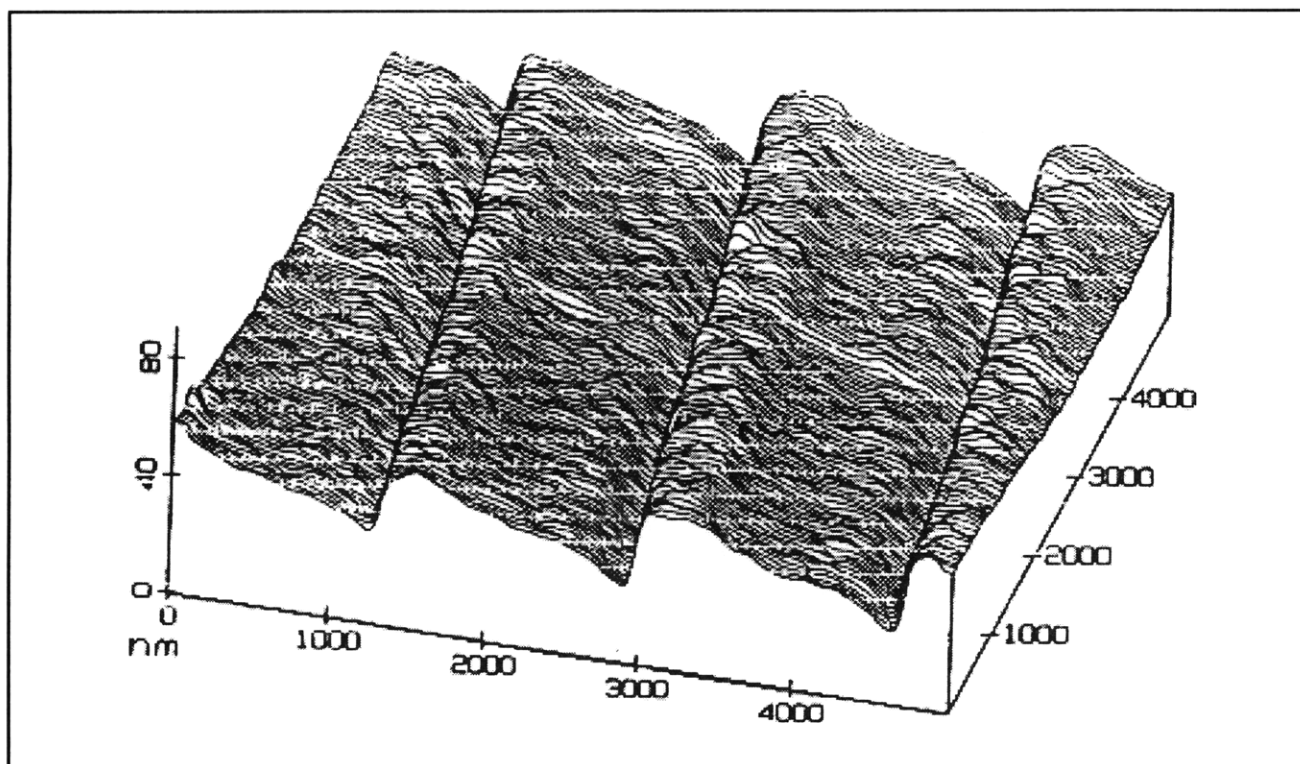

Figure 48. An AFM image of a blazed x-ray reflection grating fabricated by anisotropic etching of special off-cut (111) silicon wafers. Note the improvement of grating surface flatness and smoothness, leading to significantly improved performance.

Our gratings are patterned using interferometric lithography with the 351.1 nm wavelength, and transferred into the substrate using tri-level resist processing, reactive-ion etching (RIE), and silicon nitride masking during the KOH etch. The narrow ($\sim 0.1\ \mu$) ridge of silicon which supports the nitride mask is removed using a novel chromium lift-off step followed by a CF_4 RIE trench etch. The result is an extremely-smooth sawtooth pattern, which is suitable for x-ray reflection after applying a thin evaporative coating of Cr/Au (see figure 48).

Potential applications of these improved gratings are for laboratory and satellite-based high-resolution x-ray spectroscopy. In the current phase of the work, grating samples will be tested with special x-ray spectrometers in the laboratories of our collaborators at Columbia University and the Lawrence Berkeley National Laboratory. The next phase of the work will attempt to produce gratings on lightweight substrates suitable for astrophysical use.

4.20 Transmission Gratings as UV-blocking Filters for Neutral Atom Imaging

Sponsor

Los Alamos National Laboratory
Contract E57800017-9G

Project Staff

Dr. Joost van Beek, Robert C. Fleming, Jeanne M. Porter, Jane D. Prentiss, Robert D. Sisson, Professor Claude R. Canizares, Dr. Mark L. Schattenburg, Professor Henry I. Smith

Neutral atom beam imaging detectors are used to study dilute plasmas in laboratory systems such as tokamaks, and in astrophysical environments such as the magnetospheric region of the Earth. Neutral atom emission can be a particularly useful probe of plasmas since neutrals travel in straight lines of sight, unperturbed by electromagnetic fields.

Charge-exchange interactions between Solar wind particles and atoms in the Earth's tenuous outer atmosphere are predicted to form strong currents of neutral atoms (mostly oxygen and helium) emanating from the Earth, which, if they could be

imaged, would provide unprecedented real-time mapping of this complicated magnetohydrodynamic environment. This information would be valuable in order to safeguard the health of orbiting satellites, and ensuring the stability of our nation's electric power grid.

Unfortunately, sensitive orbiting neutral-beam detectors are easily overwhelmed by the bright flux of UV photons typically emitted from astrophysical plasmas (mostly the 121.6 nm emission from hydrogen and the 58.4 nm emission from helium). Filters which allow the passage of low-energy neutral atoms but block UV light are essential for the performance of this instrumentation. Through several years of collaboration with Los Alamos National Laboratory (LANL), the University of West Virginia, and the University of Southern California, we have developed neutral beam filters which consists of mesh-supported 200 nm-period gold transmission gratings with 50-60 nm wide slots. The tall, narrow slots in the gratings behave as lossy waveguides at or below cutoff, providing discrimination on the order of millions between UV and atoms.

We are under contract to deliver to Southwestern Research Institute (SRI) a quantity of flight grating filters for the Medium Energy Neutral Atom (MENA) instrument on the NASA Magnetospheric Imaging Medium-Class Explorer (IMAGE) mission, scheduled for launch in 1998. The gratings are fabricated by interferometric lithography with tri-level resist, followed by cryogenic reactive-ion etching and gold electroplating. An additional masking step followed by nickel plating fabricates the mesh support structure, and a final chemical etching step yields mesh-supported gratings suitable for space use.

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