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A 0.6V 2.9 μ W Mixed-Signal Front-End for ECG Monitoring

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Abstract

This paper presents a mixed-signal ECG front-end that uses aggressive voltage scaling to maximize power-efficiency and facilitate integration with low-voltage DSPs. 50/60Hz interference is canceled using mixed-signal feedback, enabling ultra-low-voltage operation by reducing dynamic range requirements. Analog circuits are optimized for ultra-low-voltage, and a SAR ADC with a dual-DAC architecture eliminates the need for a power-hungry ADC buffer. Oversampling and $\Delta\Sigma$ -modulation leveraging near- V_T digital processing are used to achieve ultra-low-power operation without sacrificing noise performance and dynamic range. The fully-integrated front-end is implemented in a 0.18 μ m CMOS process and consumes 2.9 μ W from 0.6V.

Introduction

Symptoms of cardiovascular disease are often very intermittent, necessitating ultra-low-power wearable ECG monitors with long lifetimes. In order to minimize system power, digital signal processing (DSP) can accomplish feature extraction and data compression which reduces the power burden of data transmission or storage. Recent biomedical DSPs leverage voltage scaling (down to 0.5V) to improve energy-efficiency [1]. Additional size and power benefits can be obtained by integrating the analog front-end (AFE) with the DSP back-end [2]. However, current AFEs rely on high supply voltages [3, 4] to perform signal conditioning and accommodate aggressors like electrode offset (EO) and power-line interference (PLI), limiting their compatibility with low-voltage DSPs. Therefore, this paper presents a mixed-signal front-end (MSFE) that leverages a highly-digital architecture in order to operate from a 0.6V supply which improves power-efficiency through voltage scaling, and facilitates integration with low-voltage DSPs. This work focuses on the design of ultra-low-voltage front-end analog circuits aided by configurable and energy-efficient digital processing at near- V_T operation. A highly-integrated solution is presented to demonstrate feasibility of a 0.6V system.

System Description

Supply voltage scaling is an effective way to achieve linear and quadratic power reduction in analog and digital circuits respectively. However, for ECG acquisition, PLI can be a limiting factor for voltage scaling. For example, 5mV_{p-p} of PLI with 40dB of front-end gain could easily saturate a sub-1V system before digitization by the ADC. Therefore, the system architecture in this work is based on [4], but uses $\Delta\Sigma$ -modulation to simultaneously achieve a larger PLI cancellation range and low-noise performance as a key enabler for ultra-low-voltage operation. The burden of signal processing is shifted to the digital domain which is suitable for low-voltage systems. Compared to [4], this work reduces the supply voltage from 1.5V to 0.6V and optimizes analog circuits for ultra-low-voltage operation.

Shown in Fig. 1, a low-noise amplifier (LNA) gains the input by 34.5dB, and ac-coupling achieves greater than ± 300 mV of EO rejection as required [5]. A *sinc* anti-aliasing filter (SAAF) provides an integrate-and-dump function at a sampling frequency of $f_s=10$ kHz, resulting in a *sinc* frequency response with notches placed at multiples of f_s which are precisely in the center of the aliasing bands. At the end of each integration period, the signal is digitized by a 9b dual-DAC SAR ADC.

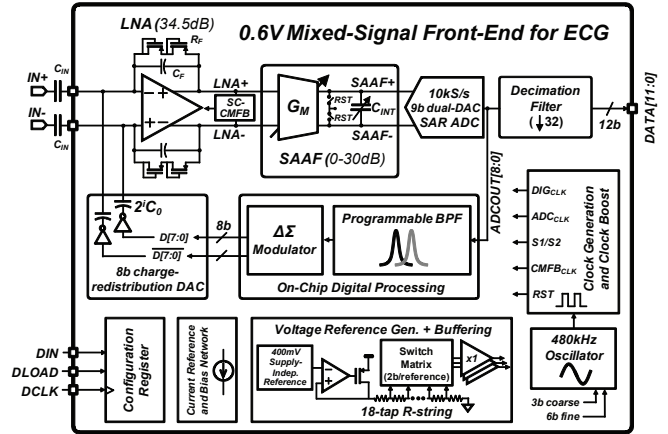


Fig. 1. System block diagram of the 0.6V MSFE for ECG.

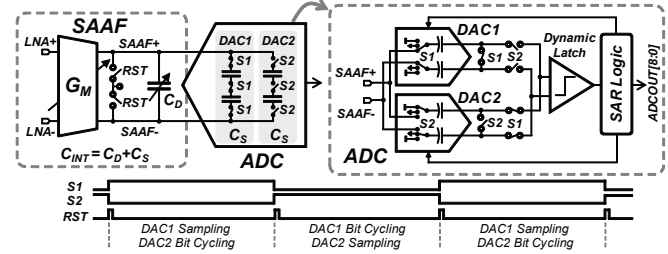


Fig. 2. SAAF and ADC block and timing diagrams.

Any PLI in the signal is captured by a programmable digital band-pass filter (BPF) and fed back to the input with an 8b charge-redistribution DAC, cancelling PLI right at the input to enable low-voltage operation. Moreover, this mixed-signal topology creates an extremely sharp and tunable notch without large passives required in purely analog systems. Since the frequency content of ECGs is well below 100Hz, $\Delta\Sigma$ -modulation and oversampling at 10kS/s are exploited to achieve greater than 12mV_{p-p} of PLI cancellation without introducing significant quantization noise with an 8b DAC. A decimation filter removes out-of-band noise and reduces the data rate down to 312.5S/s, providing up to 10.8 ENOB at the output. All reference voltages are generated by 2b R-string DACs whose reference comes from a 400mV supply-independent reference, and an on-chip oscillator and clock generator produce all clock phases.

Low-Voltage Mixed-Signal Circuit Design

The LNA is fully-differential to maximize signal range, and uses passive feedback to accurately set gain and ensure good linearity at 0.6V. Although the CMRR is limited to 70dB by using passive feedback, the CMRR requirements are relaxed since the mixed-signal notch in this system filters out PLI. Switched-capacitor common-mode feedback (SC-CMFB) is used to avoid distortion from the CMFB loop with large signal swing at low voltage. Although SC-CMFB introduces spikes at the switching frequency of 10kHz, the SAAF in this system also acts as a spike reduction filter.

In addition to anti-aliasing and spike reduction, the SAAF shown in Fig. 2 also provides a gain of $G_S = G_M / (2f_s C_{INT})$ which is digitally tunable through G_M and C_{INT} . The SAAF uses negative feedback to implement a linear transconductor and avoids cascoding in order to operate at 0.6V. C_{INT} is the sum of a 4b switched-capacitor C_D , and the sampling capacitance C_S , of the SAR ADC whose block diagram is shown in

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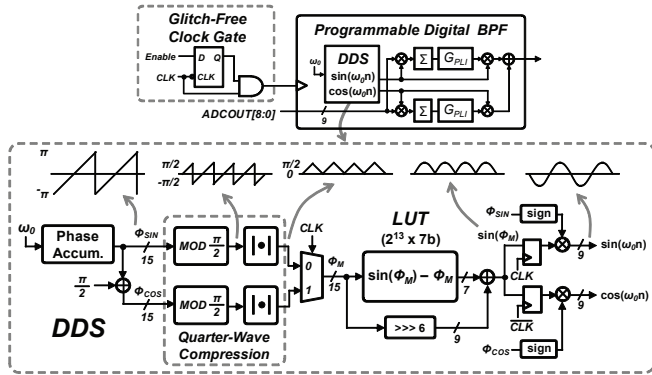


Fig. 3. Block diagram of the programmable digital BPF and DDS.

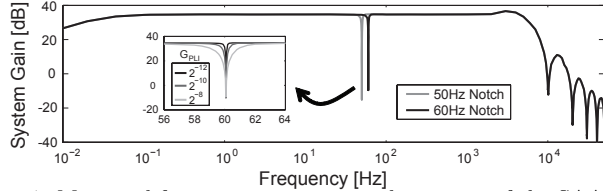


Fig. 4. Measured frequency response at the output of the SAAF.

Fig. 2. The ADC uses dual capacitive DACs, where switches $S1$ and $S2$ are complementary so that DAC1 and DAC2 alternate between bit cycling and sampling so that only one of them adds C_S to C_D during any given period. The interleaved dual-DAC architecture effectively merges the ADC sampling capacitance with the SAAF integrating capacitor, eliminating the need for a power-hungry ADC buffer which is usually needed to drive the input capacitance of a conventional SAR ADC. Finally, the ADC full-scale is digitally tunable, providing up to 4.9dB of embedded gain.

Fig. 3 shows the block diagram of the programmable digital BPF based on [4], but optimized for area and integrated for near- V_T operation. The BPF takes the form of a frequency-translated accumulator, and its center frequency and width are tunable through ω_0 and G_{PLI} respectively. In this work, the sinusoids required for frequency translation are generated on-chip using a direct-digital synthesizer (DDS) with 9b outputs, comprising a phase accumulator and a LUT as a phase to waveform generator. The number of bits in the LUT is reduced by over $5\times$ when compared to [4] by storing only a quarter period and using the sine-phase difference technique [6], requiring only 4K gates. The cosine phase is generated by adding an offset of $\pi/2$ and the LUT is used for both sine and cosine by time-multiplexing.

Measurement Results

A prototype was fabricated in a $0.18\mu\text{m}$ CMOS process. The closed-loop frequency response of the SAAF output shown in Fig. 4 demonstrates the digital programmability of the PLI notch frequency and width. The total gain of the system can be set between 34.5dB and 69.4dB by selecting one of the 60 SAAF and 4 ADC gain settings. At the lowest gain setting, the MSFE can accommodate PLI up to 12.6mV_{p-p} and an input of 8mV_{p-p} with 1% THD, meeting the requirement in [5]. The LNA alone achieves a noise-efficiency-factor (NEF) of 5.32 using a 3dB bandwidth of 2.93kHz and $9.26\mu\text{V}_{rms}$ of noise integrated from 0.5Hz to 50kHz. Using the power-efficiency-factor (PEF) introduced in [7] to account for the impact of supply voltage scaling, the LNA achieves a PEF of 17. By including the entire signal chain (LNA/SAAF/ADC/decimator), the MSFE achieves an input-referred noise of $3.44\mu\text{V}_{rms}$ in a 156Hz bandwidth, well within the $50\mu\text{V}_{p-p}$ specification [5]. This corresponds to a signal dynamic range of 58dB despite 0.6V operation, made possible by oversampling and $\Delta\Sigma$ -modulation. The ADC INL/DNL, SNDR at Nyquist, and FOM are 0.55/0.48LSB, 50dB, and 37.3fJ/conversion-step re-

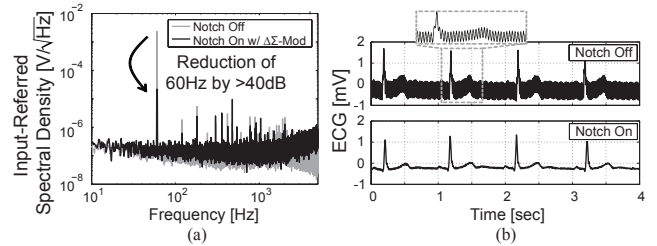


Fig. 5. Measured (a) input spectral density with a 60Hz, 8mV_{p-p} input, and (b) ECG, with the PLI notch off and on.

Technology and V_{DD}	[3] – ECG ^d 0.5 μm , 2V	[4] – ECG 0.18 μm , 1.5V	[7] – Neural 65nm LP, 0.5V	This Work – ECG 0.18 μm , 0.6V
Power/channel	3.23 μW (LNA, BPF) 4.4 μW (ADC @ 2kHz)	0.86 μW	5.04 μW	1.15 μW
Blocks included in comparison	LNA, BPF, ADC	LNA, SAAF	LNA, BPF, ADC	LNA, SAAF, ADC, Decimator, PLI filter
Power of peripheral blocks	8.5 μW	-	-	1.71 μW
Peripheral blocks included in comparison	BG ref., biasing, osc., clk gen, ADC buffer, ac-current gen	-	-	400mV ref., ref. buffers, biasing, osc., clk gen
Passband (IEC spec: 0.67-40Hz)	140Hz or 170Hz	0.12-100Hz	1-300Hz (LFP) 0.3-10kHz (spike)	0.02-156Hz
Gain	49.5, 54, 59.1, 62.3dB	37-82dB	32dB (LNA)	34.5-69.4dB
Input-referred noise (IEC spec: $50\mu\text{V}_{p-p}$ for 10s)	1.1 μV_{rms} [170Hz]	3.4 μV_{rms} [0.12-100Hz]	4.9 μV_{rms} [300Hz-10kHz]	^a 3.44 μV_{rms} [0.5-156Hz]
Maximum input range (IEC spec: 8mV_{p-p})	35 mV_{p-p}	10.8 mV_{p-p}	3.5 mV_{p-p}	8 mV_{p-p}
NEF/PEF (LNA only)	5/50	8.3/103	^c 5.99/17.96	^b 5.32/17
CMRR (IEC spec: 60dB)	> 105dB	> 60dB	75dB	> 70.4dB
Electrode offset tolerance (IEC spec: $\pm 300\text{mV}$)	> $\pm 300\text{mV}$	> $\pm 300\text{mV}$	$\pm 50\text{mV}$	> $\pm 300\text{mV}$
Maximum PLI tolerance	-	5 mV_{p-p}	-	12.6 mV_{p-p}
Area/channel	-	0.225 mm^2	0.013 mm^2	0.445 mm^2

^a Noise includes contributions from LNA, SAAF, ADC, and decimation filter.

^b NEF calculation based on $9.26\mu\text{V}_{rms}$ input-referred noise integrated over 0.5Hz-50kHz, using a 2.93kHz 3dB bandwidth.

^c Includes power and noise of LNA, BPF, and ADC.

^d [3] has features such as actively-based sampling, feature extraction, and signal integrity monitoring (power not included).

^e ADC power quoted for a 2kHz sampling rate. ECG readout channel in [3] is adaptively sampled at 64Hz or 1024Hz.

^f Includes noise of ECG readout channel and ADC at a gain setting of 62.3dB.

Measured Power Breakdown @ 0.6V		
Single Channel	LNA, SAAF, ADC, Feedback DAC	770nW
	Digital PLI filter, Digital decimation filter	180nW, 34nW
	Leakage	166nW
Total channel power (PLI notch off, on)		0.97μW, 1.15μW
Peripherals	Current reference and bias network	80nW
	400mV supply-indep. ref. and buffers	1.32 μW
	Oscillator (480kHz) and clock generation	310nW
	Total peripheral power	1.71μW
Total power (PLI notch off, on)		2.68μW, 2.86μW

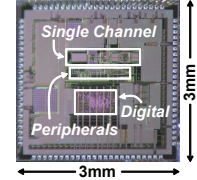


Fig. 6. Measured chip summary, die photo, and comparison table.

spectively. Fig. 5a shows the input-referred spectrum with an 8mV_{p-p} , 60Hz input. With the notch enabled, the tone is attenuated and the $\Delta\Sigma$ -modulator shapes the DAC quantization noise to higher frequencies, maintaining the in-band noise floor to achieve an interference dynamic range of 62dB using just an 8b DAC. Finally, Fig. 5b shows ECG measurements on a male subject using gel electrodes and unshielded wiring. The PLI is clearly canceled when the notch filter is enabled.

Conclusion

Fig. 6 shows the chip summary, die photo, and comparison table. At 0.6V, the single-channel MSFE consumes $1.15\mu\text{W}$, and the integrated peripheral circuits consume $1.71\mu\text{W}$. In comparison, the same implementation at a supply of 1.5V as in [4] would require greater than $5\mu\text{W}$ of additional power. The combination of a mixed-signal architecture and circuit optimizations at scaled voltages helps to achieve ultra-low-power operation at 0.6V, demonstrating compatibility with ultra-low-voltage DSPs.

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